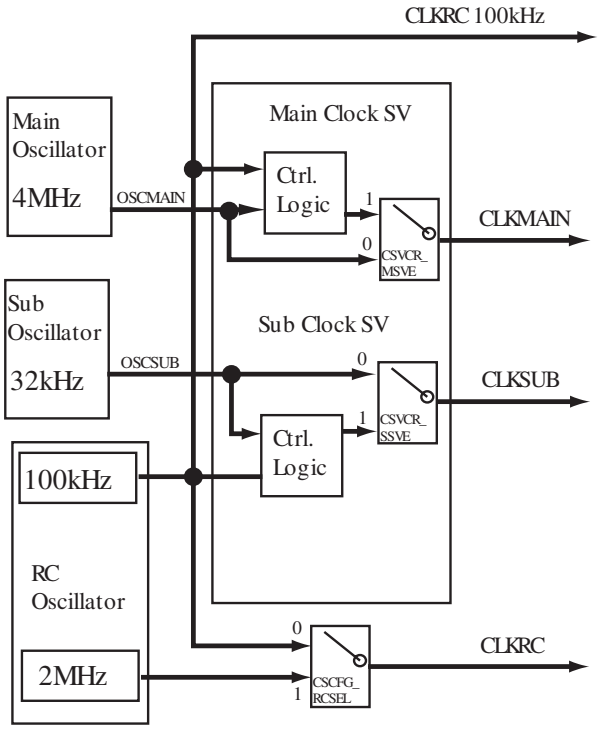
Chapter 16 Clock Supervisor

This section gives an overview of the Clock Supervisor. Purpose of the Clock Supervisor is the supervision of the Main- and Sub oscillators. In case of oscillation (OSCMAIN or OSCSUB) failure the Clock Supervisor control logic will take action, i.e. switching to an internal RC-oscillation clock (CLKRC 100kHz), depending on the operation mode set in the control register.

In MB91FV460B, MB91F467P and later devices, an new Clock Supervisor version with extended functionality is implemented. This new feature is marked with the keyword “New feature”.

1. Overview Clock Supervisor

Figure 1-1 Block diagram of the clock supervisor



The purpose of the clock supervisor is the supervision of the main and sub oscillation clocks. In case of a oscillation failure (OSCMAIN and/or OSCSUB) it can be replaced by an on-chip RC-oscillation clock (CLKRC 100kHz), depending on the configuration.

If a clock the MCU currently uses, fails for a certain time (20-80 µs for Main clock / 160-640 µs for Sub clock) the MCU is reset by Setting Initialization Request (INIT) and the reset cause can be checked after reset vector fetch.
If the Sub clock is failing while the MCU is in Main clock mode, reset can be delayed until the transition to Sub clock mode or no reset will be initiated. The user can choose the behaviour with a control bit in the Clock Supervisor Control Register.

There are two independent supervisors, one for the Main clock and one for the Sub clock. They can be enabled/disabled separately.
Main clock and Sub clock supervisor are disabled and re-enabled automatically if the corresponding oscillator is disabled and re-enabled.

If the MCU changes to STOP state, the RC-oscillator can be automatically disabled by a control bit. It will be enabled again upon wake-up from STOP state.

There are two status bits in the Clock Supervisor Control Register which indicate the failure of the Main clock and Sub clock. These bits can be available at two port pins (device dependent).
Single clock devices can use the CLKRC as Sub clock.

New feature: The two Clock Supervisor status bits can be cleared by CPU access, if the main and/or sub oscillator has resumed oscillation. The clock is switched back to OSCMAIN and/or OSCSUB in this case.

New feature: The RC oscillator is enabled in STOP mode automatically, if the Hardware Watchdog is configured to run during STOP. The RC oscillator can **only** be stopped in STOP mode, and then it depends on the Hardware Watchdog and the control bit in the Clock Supervisor Control Register.

2. Clock Supervisor Register

This section lists the Clock Supervisor Control Register and describes the function of each bit in detail.

■ Clock Supervisor Control Register (CSVCR)

The Clock Supervisor Control Register (CSVCR) sets the operation mode of the Clock Supervisor. Figure 2-1 shows the configuration of the Clock Supervisor Control Register.

Figure 2-1 Configuration Clock Supervisor Control Register (CSVCR)

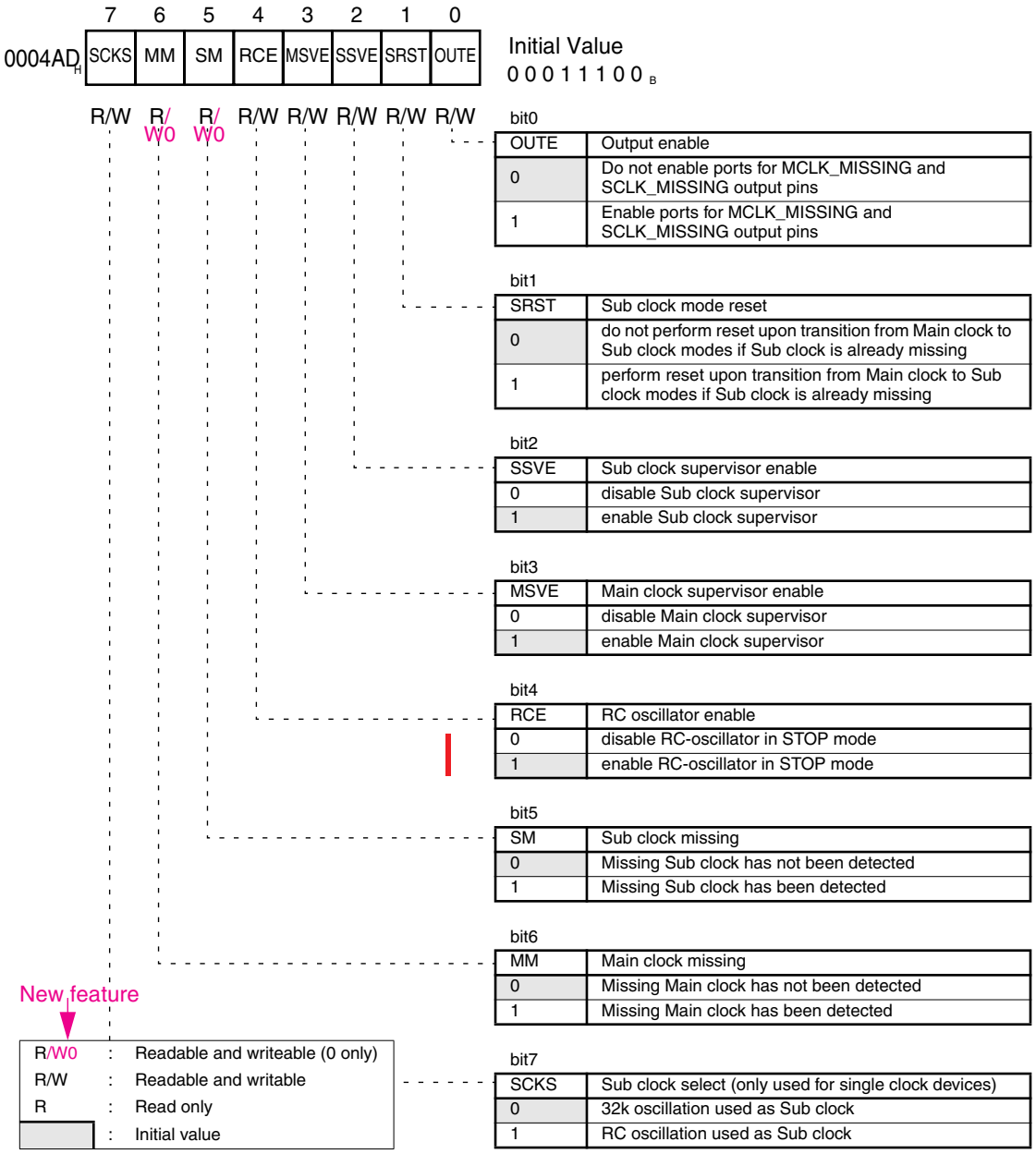


Table 2-1 describes the function of each bit of the Clock Supervisor Control Register (CSVCR).

Table 2-1 Functional Description of each bit of the Clock Supervisor Control Register

Bit	Name	Function
7	SCKS (Sub clock select)	This bit is to select between 32 kHz external oscillation and internal RC oscillation as Sub clock. If this bit is '0' then the external 32 kHz oscillation is used as Sub clock, if it's '1' then the internal RC oscillation is used as Sub clock. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.
6	MM (Main clock missing)	If this bit is 1, the Main clock supervisor has detected that the Main oscillation clock coming from X0, X1 is missing, e.g. by a broken crystal. If this bit is '0', a missing Main clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: This bit can be cleared by CPU access, if the main oscillator has resumed oscillation. If the main oscillator is still failing, the write access is ignored.
5	SM (Sub clock missing)	If this bit is 1, the Sub clock supervisor has detected that the sub oscillation clock coming from X0A, X1A is missing, e.g. by a broken crystal. If this bit is '0', a missing Sub clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: This bit can be cleared by CPU access, if the sub oscillator has resumed oscillation. If the sub oscillator is still failing, the write access is ignored.
4	RCE (RC-oscillator enable)	Setting this bit to '1' enables the RC-oscillator in STOP mode. Outside STOP mode, the RC-oscillator is always enabled. This bit is set to '1' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: If HWWD.STP_RUN (=HWWD[4]) is set in the Hardware Watchdog, then the RC oscillator is enabled and read and read-modify-write operations will return '1' independendly of RCE register setting. Effective RCE = RCE_Register or HWWD.STP_RUN
3	MSVE (Main clock supervisor enable)	Setting this bit to '1' enables the Main clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
2	SSVE (Sub clock supervisor enable)	Setting this bit to '1' enables the Sub clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
1	SRST (Sub clock mode reset)	If this bit is set to '1', a reset is performed upon transition from Main/PLL clock mode to Sub clock mode if the Sub clock is already missing. If this bit is set to '0', no reset is performed in this case. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.

Bit	Name	Function
0	OUTE (Output enable)	This bit can be used as an output enable to output the signals MCLK_MISSING (bit 3 of CSVCR) and SCLK_MISSING (bit 4 of CSVCR) to port pins. For more information about the pins see the corresponding Datasheet. If this bit is set to '1', the ports are enabled for MCLK_MISSING and SCLK_MISSING output. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.

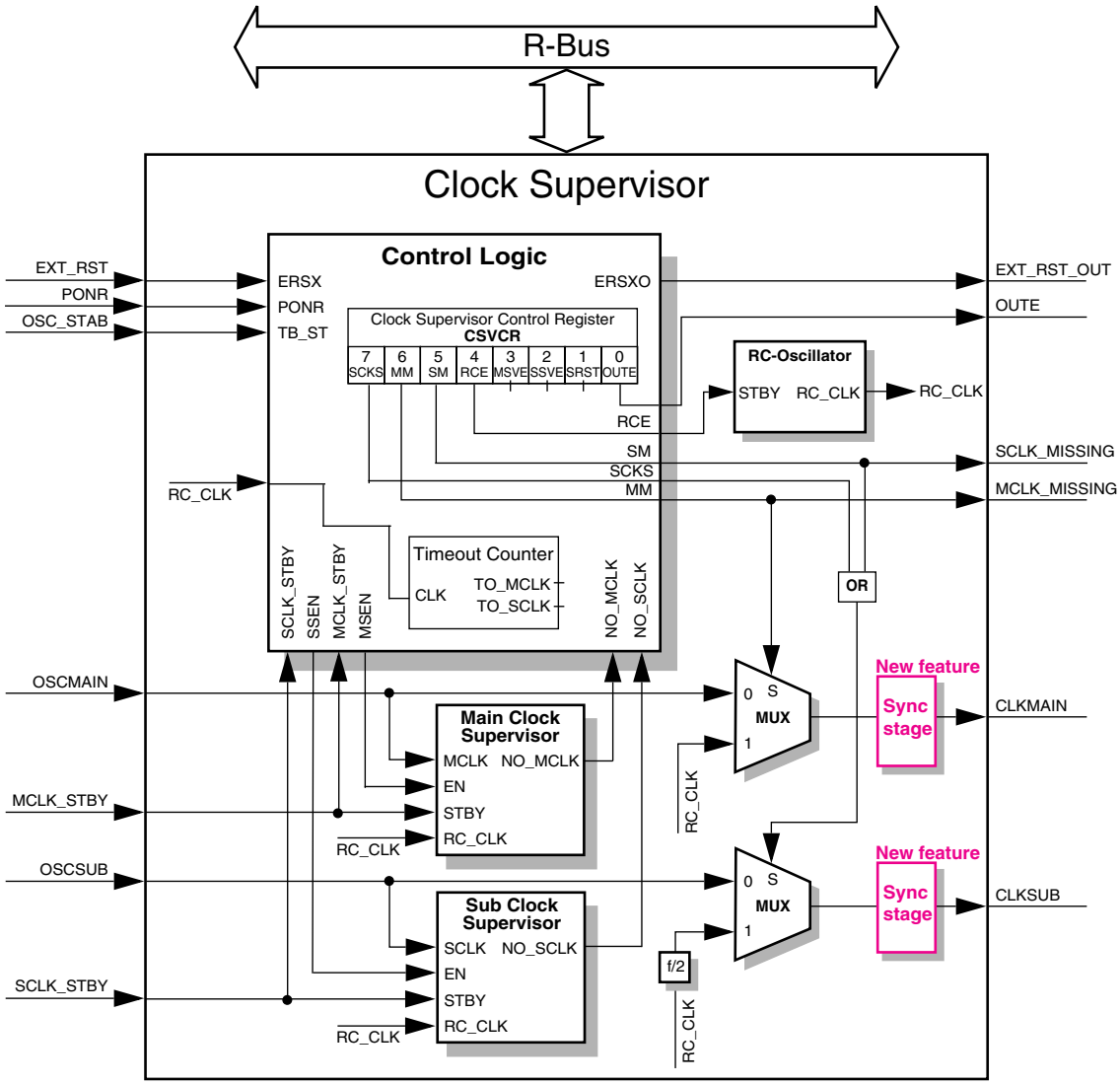
3. Block Diagram Clock Supervisor

This section presents a block diagram of the Clock Supervisor. The building blocks of the Clock Supervisor are:

- Main Clock Supervisor
- Sub Clock Supervisor
- Control Logic
- RC-Oscillator

■ Block Diagram Clock Supervisor

Figure 3-1 Bock Diagram of Clock Supervisor



SCLK_OUT and MCLK_OUT can be observed using the Clock Monitor Module. SCLK_MISSING and MCLK_MISSING can be programmed to device specific outputs (see the datasheet of the used device for the information which pins are used) by setting OUTE=1.

Signal EXT_RST_IN is the reset input, connected to the external INITX pin.
Signal EXT_RST_OUT is the reset output and causes Setting Initialization Request (INIT).

4. Operation Modes

This section describes all operation modes of the Clock Supervisor.

■ Operation mode with initial settings

In case the clock supervisor control register (CSVCR) is not configured at the beginning of the user program, the RC-oscillator, the Main clock supervisor and the Sub clock supervisor is enabled.

- The RC-oscillator is enabled at power-on.
- The Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing before the completion of the ’oscillation stabilization wait time’, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC. If the Main clock is missing from power-on, the power-on reset state is never left, which in this case is a safe state. The user must make sure with external pull-up/pull-down resistors that all relevant signal are pulled to the correct level.
- The Sub clock supervisor is enabled after the completion of the ’Sub clock timeout’ (TO_SCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- If the Main clock stops while the Main clock supervisor is enabled, the Main clock is replaced with CLKRC 100kHz, the MM bit is set to ’1’ and reset (EXT_RST_OUT) is asserted.
- If the Sub clock stops and the Sub clock supervisor is enabled, the behaviour depend on whether the MCU is in Main clock mode or in Sub clock mode. If the Sub clock stops in Sub clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to ’1’ and reset (EXT_RST_OUT) is asserted. If the Sub clock stops in Main clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to ’1’ and no reset occurs upon transition to Sub clock mode, since the SRST bit has its initial value of ’0’. If the SRST bit is ‘1’ a reset (INIT) occurs.

Figure 4-1 Timing Diagram: Initial settings, Main clock missing during power-on reset

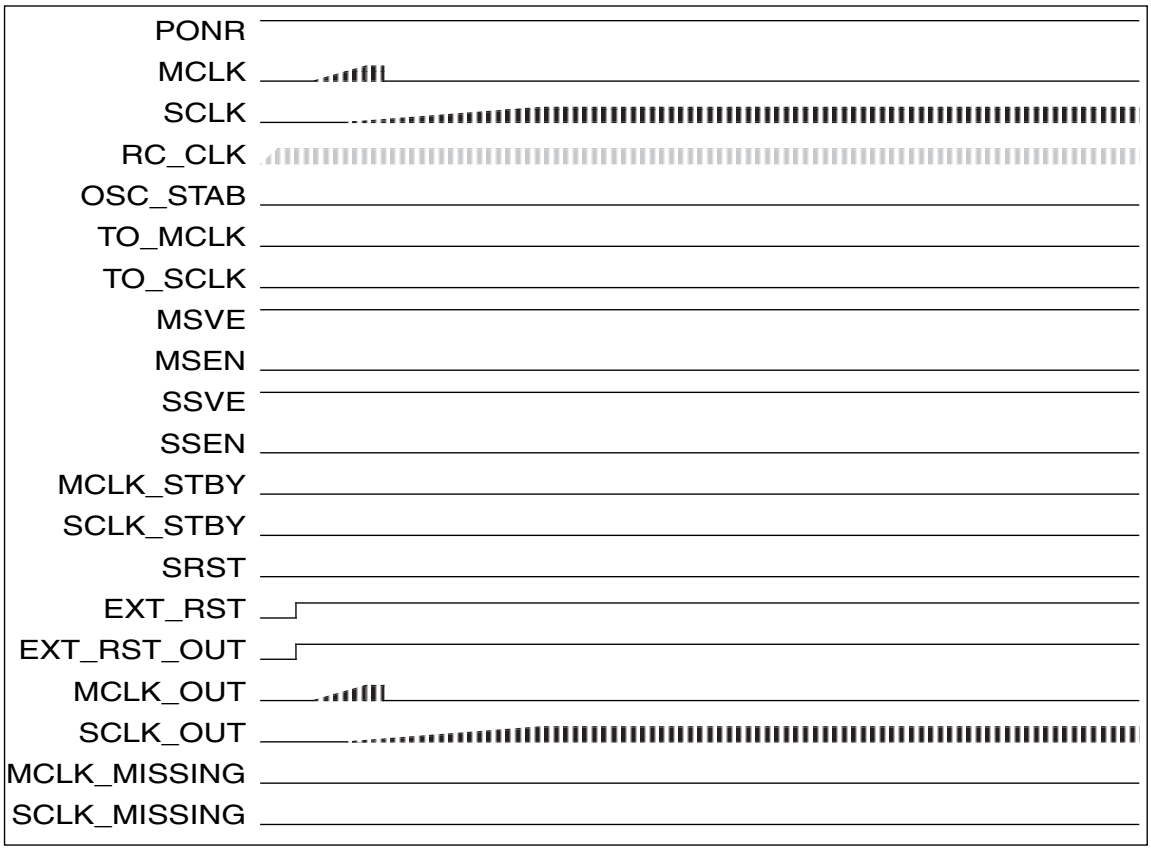


Figure 4-2 Timing Diagram: Initial settings, Main clock missing during 'oscillation stabilization wait time'

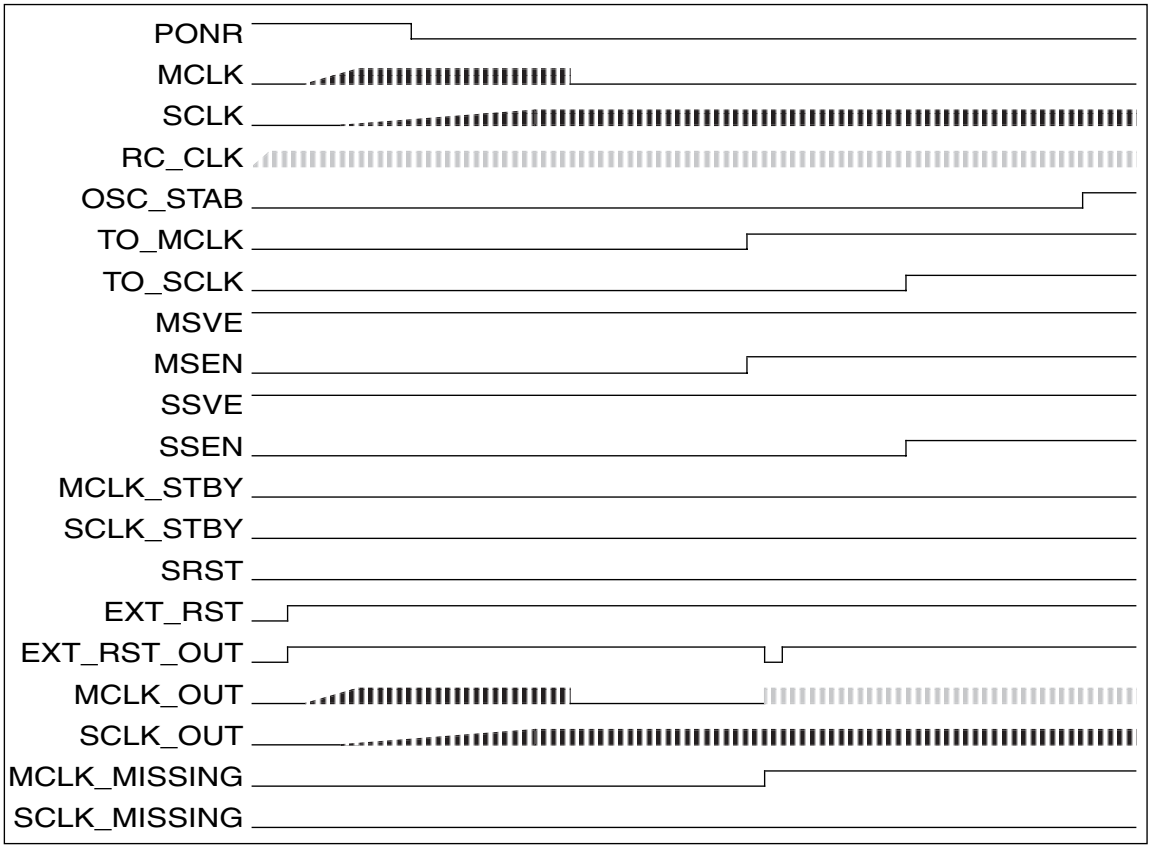


Figure 4-3 Timing Diagram: Initial settings, Main clock missing after 'oscillation stabilization wait time'

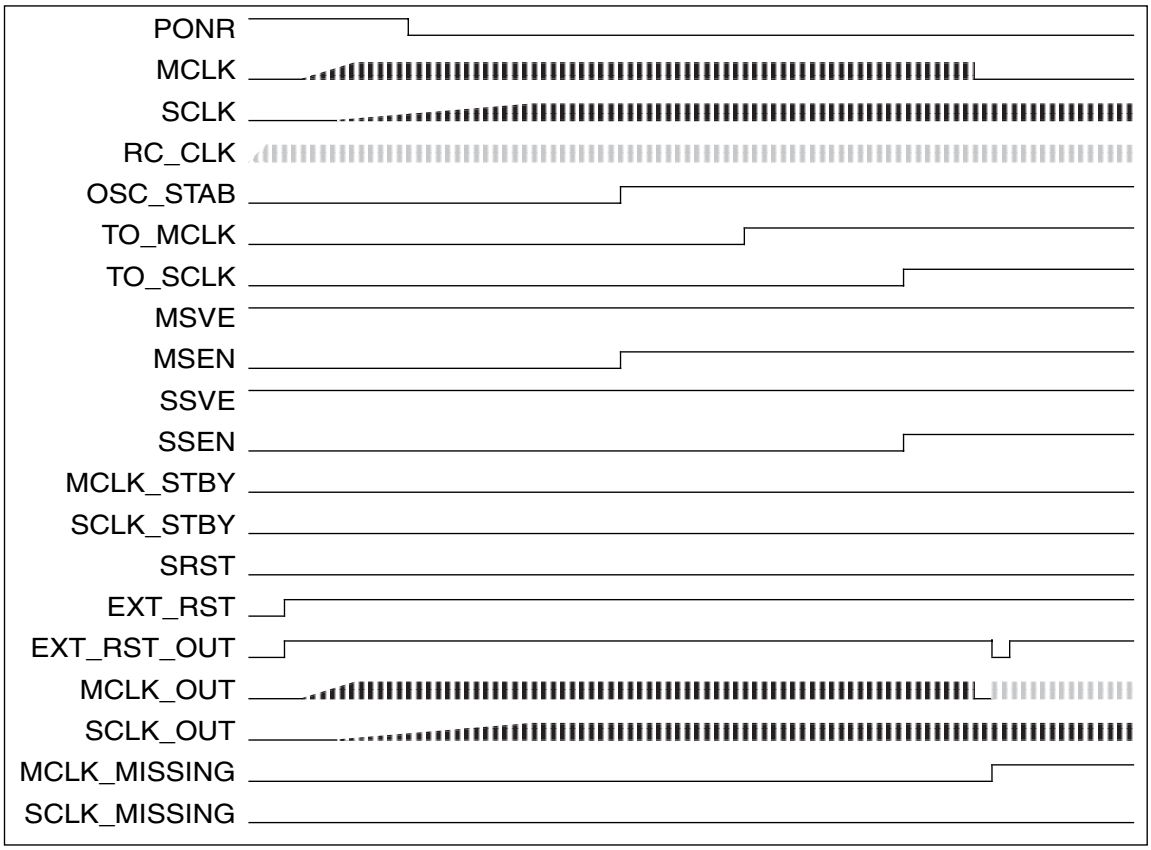


Figure 4-4 Timing Diagram: Initial settings, Sub clock missing before timeout

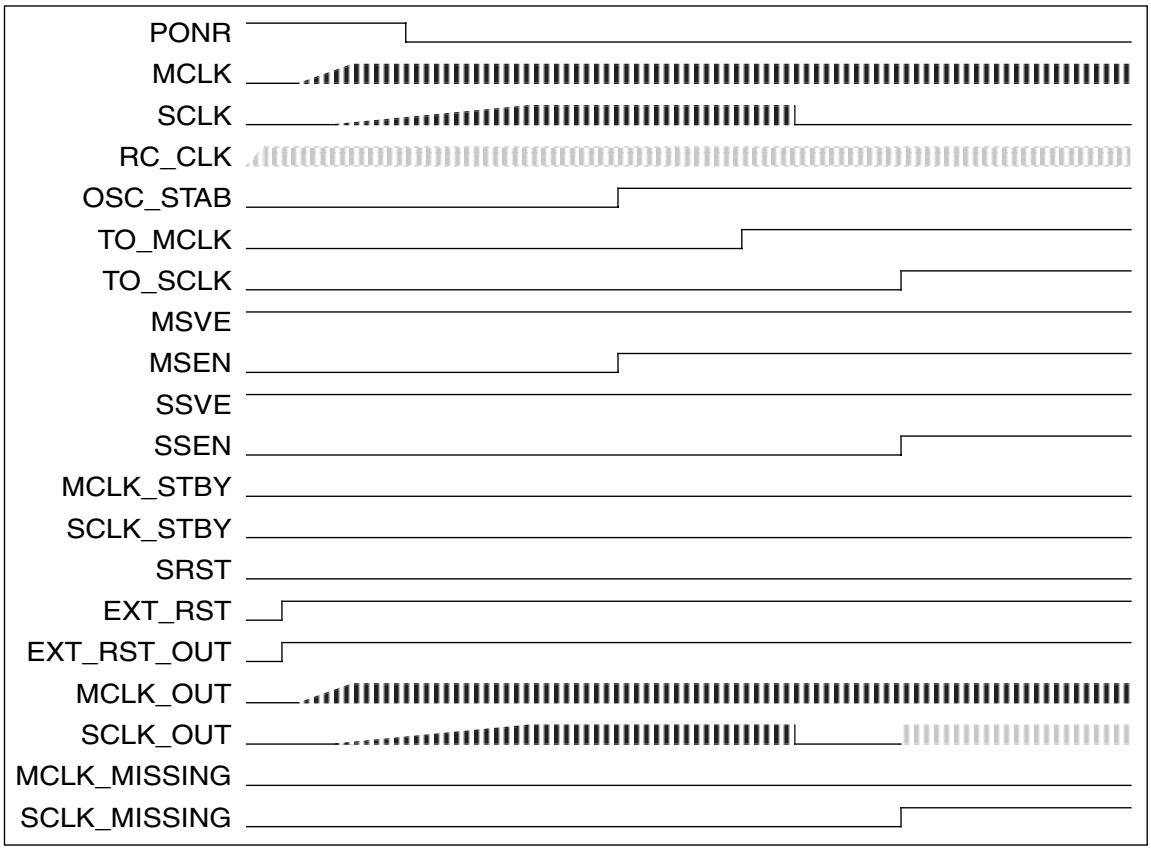
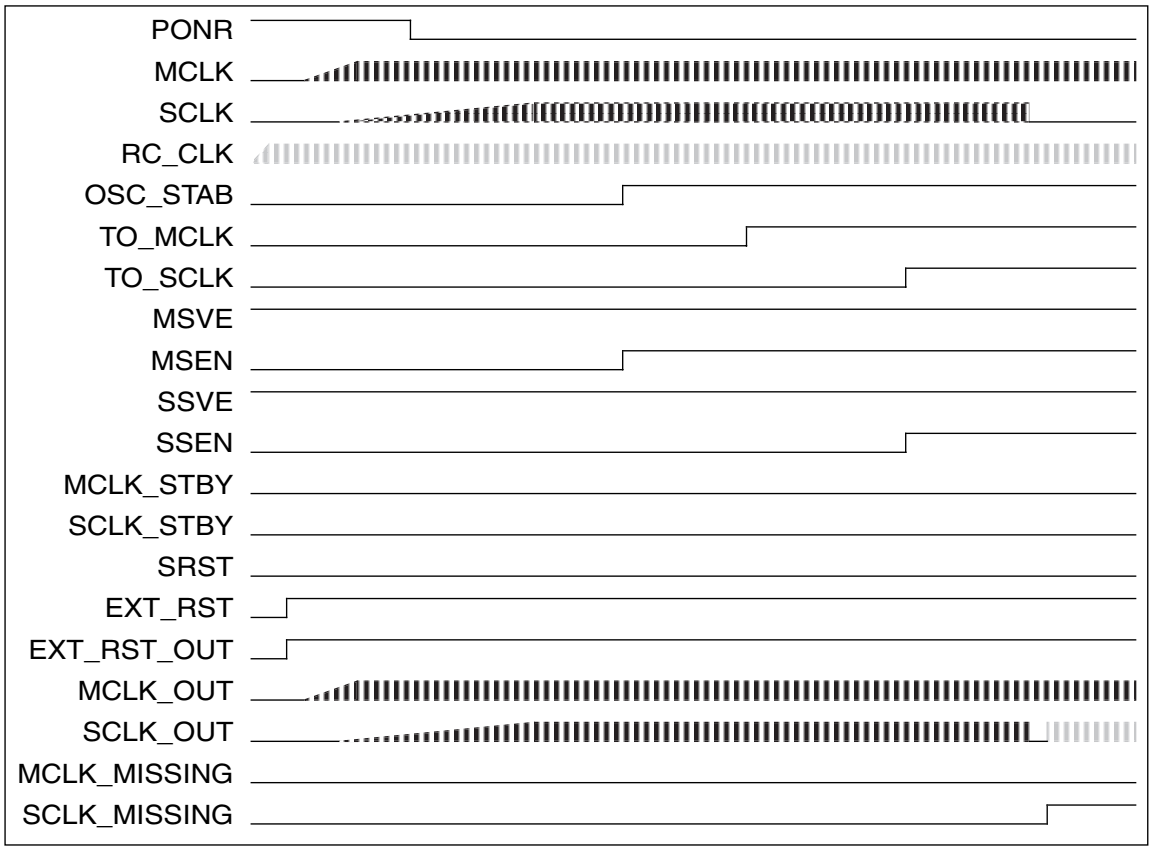


Figure 4-5 Timing Diagram: Initial settings, Sub clock missing after timeout

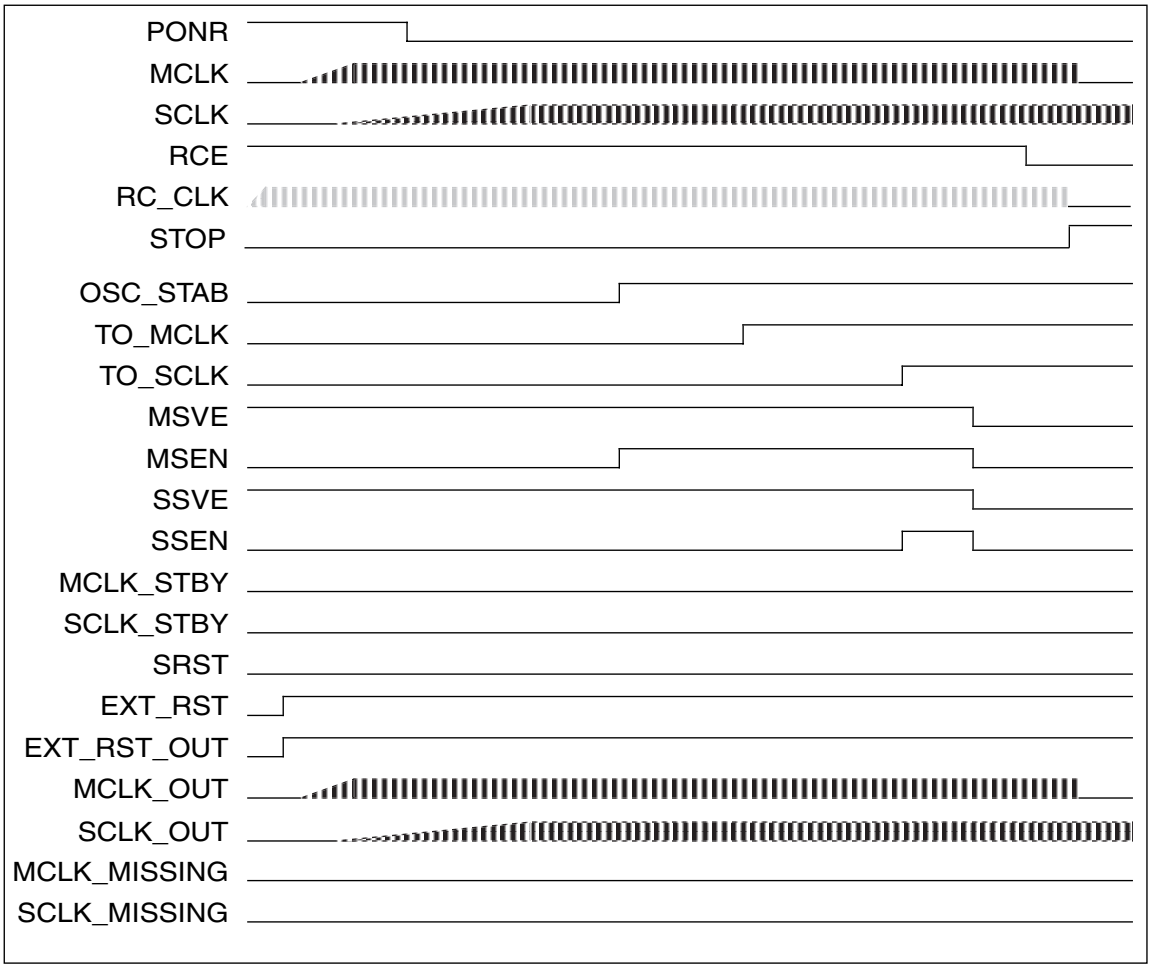


■ Disabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and Main clock or Sub clock supervisor is enabled.

- The RC-oscillator can be disabled only in STOP mode.
  First check that both SM and MM (bit 5 and bit 6 of CSVCR) are ’0’.
  Then disable the RC-oscillator by setting RCE to ’0’. If either SM or MM bit is ’1’, RCE must not be set to ’0’.
- New feature: If the Hardware Watchdog is to run in STOP mode (HWWD.STP_RUN=’1’) then the RC-oscillator is enabled by hardware.
- The Main clock supervisor is disabled by setting MSVE (bit 3 of CSVCR) to ’0’.
- The Sub clock supervisor is disabled by setting SSVE (bit 2 of CVSVR) to ’0’.

Figure 4-6 Timing Diagram: Disabling the RC-oscillator and the clock supervisors

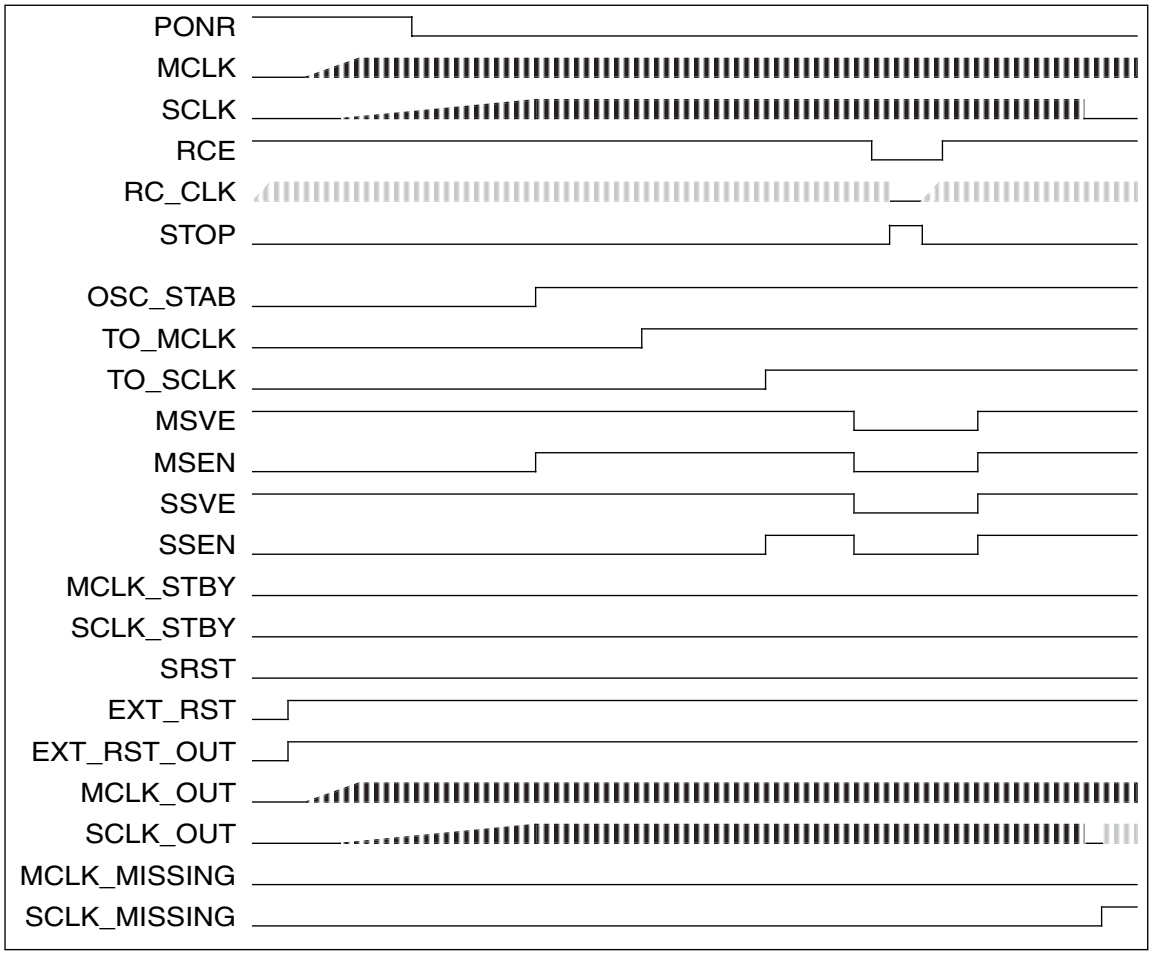


■ Re-enabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and both Main clock and Sub clock supervisor are disabled.

- The RC-oscillator is always enabled in RUN state. It can only be disabled in STOP, and after wakeup from STOP it will re-start automatically.
- The Main clock supervisor is enabled by setting MSVE (bit 3 of CSVCR) to ’1’.
- The Sub clock supervisor is enabled by setting SSVE (bit 2 of CSVCR) to ’1’.

Figure 4-7 Timing Diagram: Re-enabling the RC-oscillator and the clock supervisors



■ New feature: Switching back from RC to Main Oscillation

The initial point of this scenario is that the Main clock was missing, the Main clock supervisor has set the MM flag and switched to RC clock. The CPU already got reset (INIT) from clock supervisor and has detected MM=1 as reset source (See "Check if reset was asserted by the Clock Supervisor" on P. 240). The user is quite sure that the Main clock returned meanwhile or will return soon and wants to switch back to Main clock.

- The MM flag can be cleared by writing ‘0’ (bit 6 of CSVCR).
- If the Main clock is still missing during the write access, the write operation has no effect, the MM flag keeps ‘1’ value and the clock supervisor continues giving out RC clock.
- If the Main clock is operating during the write access, the MM flag is cleared and the clock is switched back to Main clock via a synchronisation stage.
- It is possible to poll the MM flag until the Main clock is resumed:

```
        ldi       #_csvcr,r1
  clear_CSV_loop:
        bandh     #0b1001,@r1      ;; Clear MM+SM
        btsth     #0b0110,@r1      ;; Check: Is one of them 1?
        bne       clear_CSV_loop
```

■ New feature: Switching back from RC to Sub Oscillation

The initial point of this scenario is that the CPU is running on Sub clock and Sub clock was missing. The Sub clock supervisor has set the SM flag and switched to RC clock (divided by 2). A clock supervisor reset was not generated because of CSVCR.SRST was ‘0’. Now the CPU is running user software on RC clock. The flag SM=1 was found by polling. The user is quite sure that the Sub oscillation returned meanwhile or will return soon and wants to switch back to Sub oscillation.

- The SM flag can be cleared by writing ‘0’ (bit 5 of CSVCR).
- If the Sub clock is still missing during the write access, the write operation has no effect, the SM flag keeps ‘1’ value and the clock supervisor continues giving out RC clock.
- If the Sub clock is operating during the write access, the SM flag is cleared and the clock is switched back to Sub clock via a synchronisation stage.
- It is possible to poll the SM flag like described in the Main clock example above.

■ Sub clock modes

The Main clock supervisor is automatically disabled in Sub clock modes. The enable bit MSVE remains unchanged. At transition from Sub clock mode to Main clock mode the Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing before the completion of the 'oscillation stabilization wait time', after the 'Main clock timeout' (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.

■ Changing the behaviour upon transition to Sub clock mode if the Sub clock has already stopped in Main clock mode

If the Sub clock has stopped in Main clock mode and this was detected by the Sub clock supervisor, the behaviour upon transition to Sub clock mode depends on the state of the SRST bit.

- If SRST is set to '0' (initial value), reset is not asserted at the transition to Sub clock mode. The transition is performed using the RC-oscillation clock as Sub clock. In this case it is recommended to check the SM bit before the transition to Sub clock mode to get the information if Sub clock or CLKRC is used.
- If SRST is set to '1', reset is asserted at the transition to Sub clock mode.

The following timing diagrams (Figure 4-8, Figure 4-9, Figure 4-10) illustrate this behaviour.

Figure 4-8 Timing Diagram: Sub clock missing in Main clock mode, SRST=0

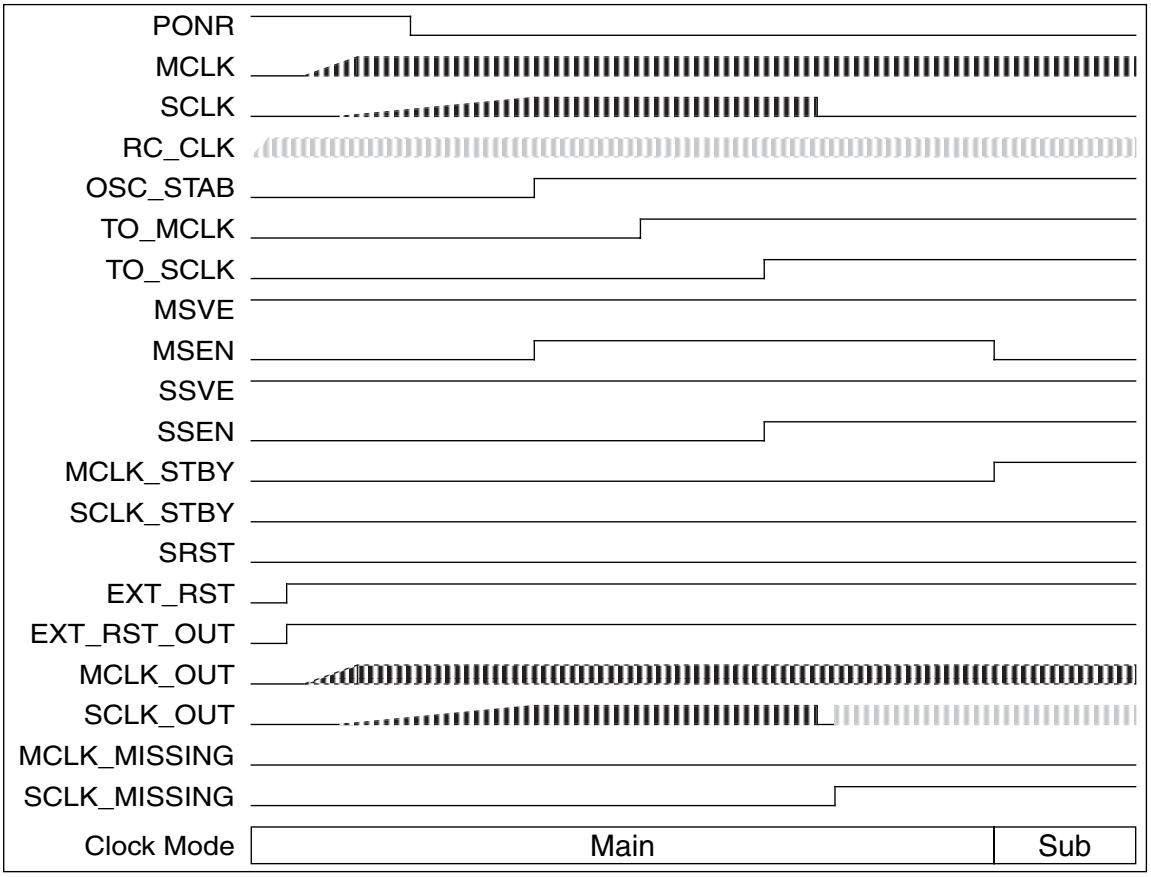


Figure 4-9 Timing Diagram: Sub clock missing in Main clock mode, SRST=1

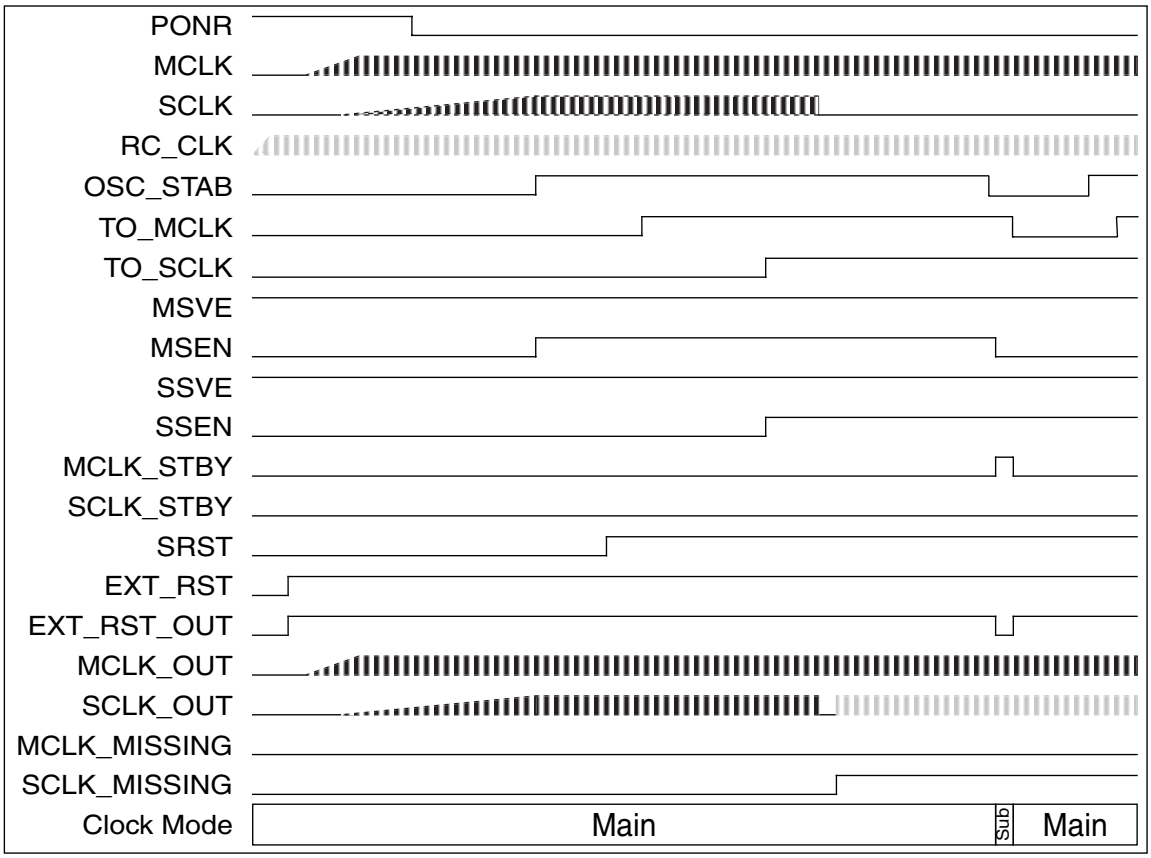
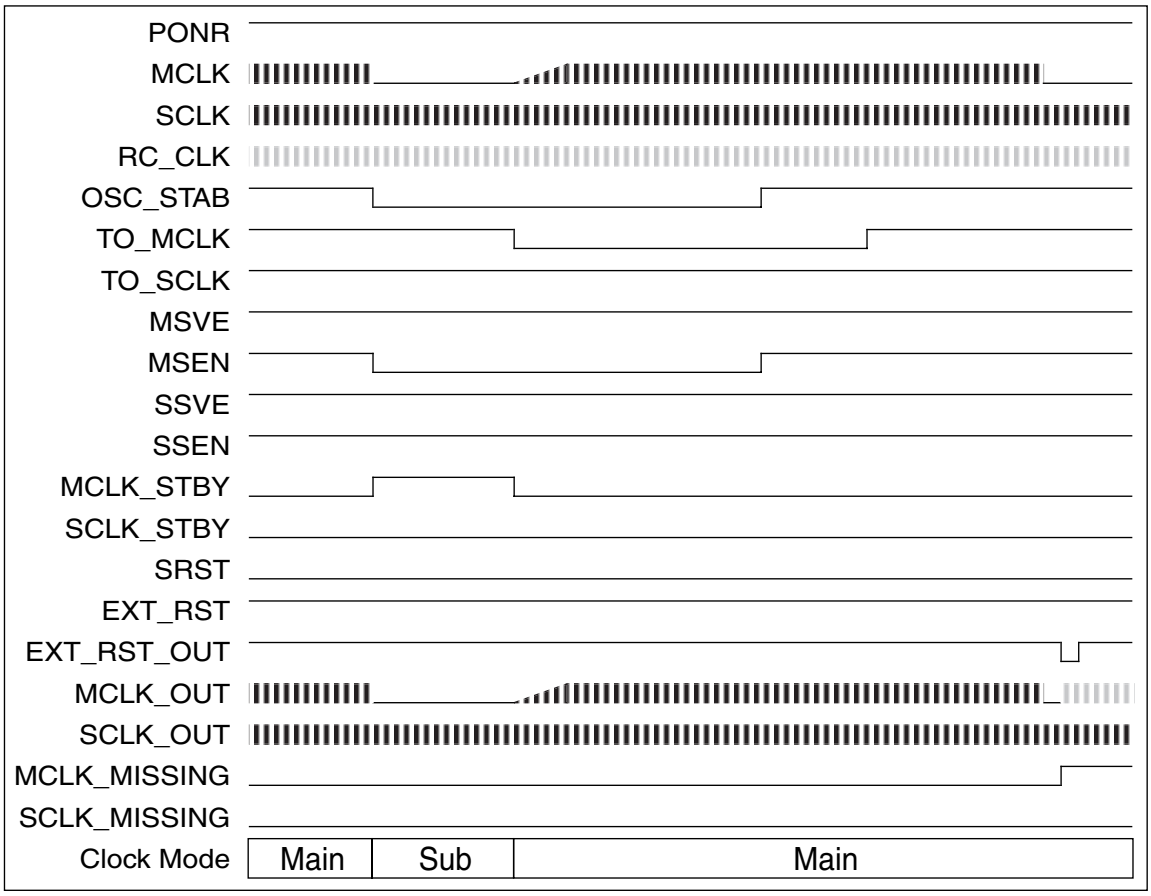


Figure 4-10 Timing Diagram: Waking up from Sub clock mode



■ STOP mode (with both oscillators disabled)

In this section, “STOP mode” means that the CPU is in STOP state and both oscillators are disabled by setting STCR.OSCD1=’1’ and STCR.OSCD2=’1’. The Clock Supervisor’s inputs MCLK_SBY and SCLK_SBY are connected to the oscillator disable lines OCSD1 and OSCD2, respectively.

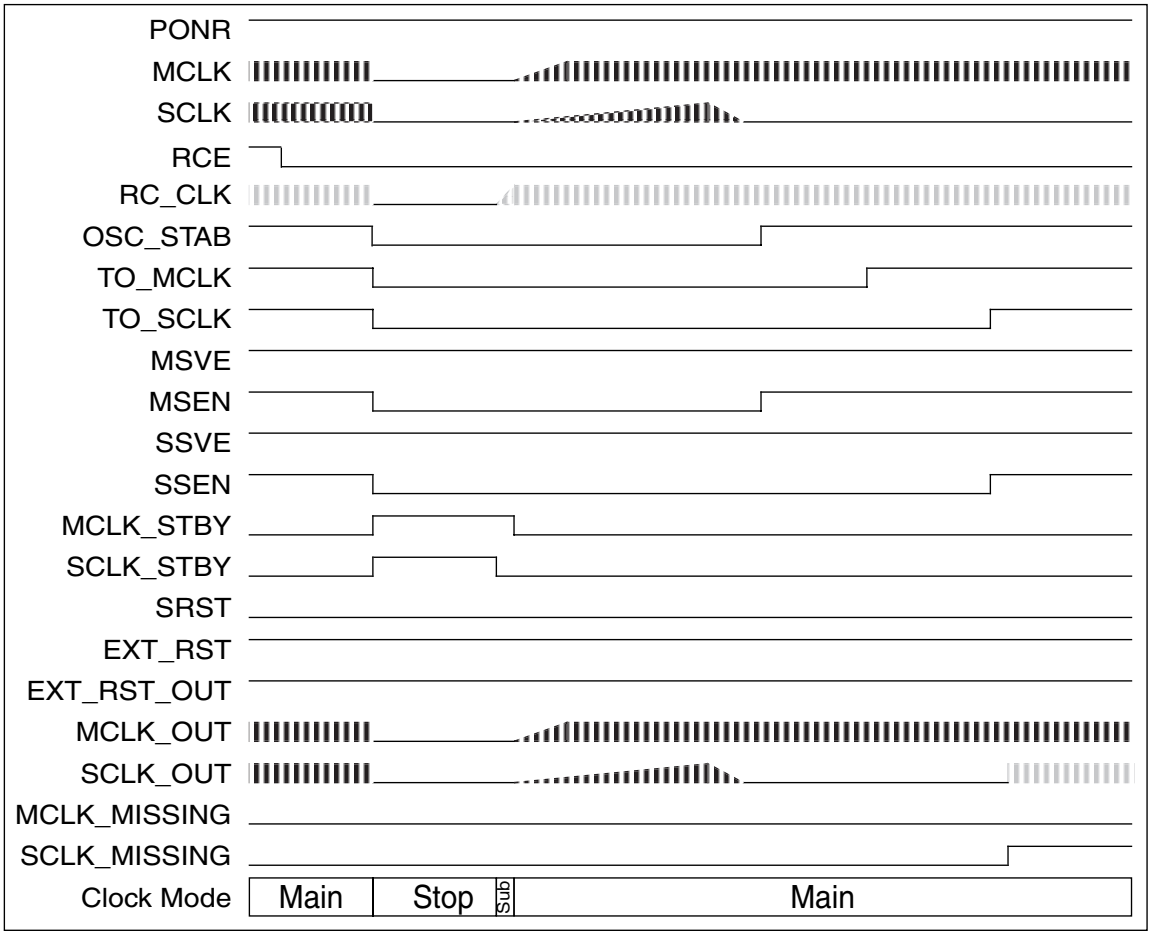
If Main clock and Sub clock supervisors are enabled, they will be automatically disabled at transition into STOP state. The corresponding enable bits in the clock supervisor control register remain unchanged. So after wake-up from STOP mode the clock supervisors will be enabled again. If the corresponding enable bits are set to ’0’, the clock supervisors will stay disabled after wake-up from STOP mode.

The RC-oscillator is disabled in STOP, if the RCE bit in the CSVCR register is cleared.

New feature: If the Hardware Watchdog is enabled in STOP state (HWWD.STP_RUN=’1’), then the RC-oscillator is enabled by hardware during STOP. The RCE bit is unchanged, but read and read-modify-write operations return ‘1’.

- The RC-oscillator is enabled immediately after wake-up from STOP mode.
- The Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing after wake-up from STOP mode, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- The Sub clock supervisor is enabled after the ’Sub clock timeout’ (TO_SCLK) from the timeout counter which is clocked with the CLKRC.

Figure 4-11 Timing Diagram: Waking up from STOP state



■ RTC mode (STOP mode with Real Time Clock enabled)

In this section, “RTC mode” means that the CPU is in STOP state and one of the quartz oscillators is enabled by setting STCR.OSCD1=’0’ or STCR.OSCD2=’0’. The enabled oscillator clock is switched to the Real Time Clock to keep it running during STOP. The behavoiur of the Clock Supervisor depends on several settings.

- If the RTC is connected to Main clock, the behaviour of the main clock supervisor is like described in Table 4-1

Table 4-1 Main Clock Supervisor in RTC mode.

RC oscillator enable CSVCR.RCE	Main Oscillator disable STCR.OSCD1	Main clock supervisor enable SVCR.MSVE	Behaviour in STOP mode if Main clock fails and the RTC is connected to Main clock
1	1	X	Main clock fail cannot be seen because the Main oscillator is disabled. The Main clock supervisor is disabled because of the Main oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set MM flag, switch the Main clock to RC clock and generate an reset (INIT) to CPU. The STOP mode is cancelled by the reset. The RTC is initialized by the reset.
1	0	0	Main clock supervisor is disabled by MSVE=0. In case of Main clock fail, the RTC clock simply stopps.
0	X	X	Main clock supervisor is disabled because of it does not get RC clock. In case of Main clock fail, the RTC clock simply stopps.

(Note) New feature: RCE setting is valid if HWWD.STPRUN (HWWD[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

- If the RTC is connected to Sub clock, the behaviour of the sub clock supervisor is like described in Table 4-2

Table 4-2 Sub Clock Supervisor in RTC mode.

RC oscillator enable CSVCR.RCE	Sub Oscillator disable STCR.OSCD2	Sub clock supervisor enable SVCR.SSVE	Behaviour in STOP mode if Sub clock fails and the RTC is connected to Sub clock
1	1	X	Sub clock fail cannot be seen because the Sub oscillator is disabled. The Sub clock supervisor is disabled because of the Sub oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set SM flag and switch the Sub clock to RC clock.The RTC continues running on RC clock. A reset is not generated because there is no transition from Main clock to Sub clock during STOP mode.
1	0	0	Sub clock supervisor is disabled by SSVE=0. In case of Sub clock fail, the RTC clock simply stopps.
0	X	X	Sub clock supervisor is disabled because of it does not get RC clock. In case of Sub clock fail, the RTC clock simply stopps.

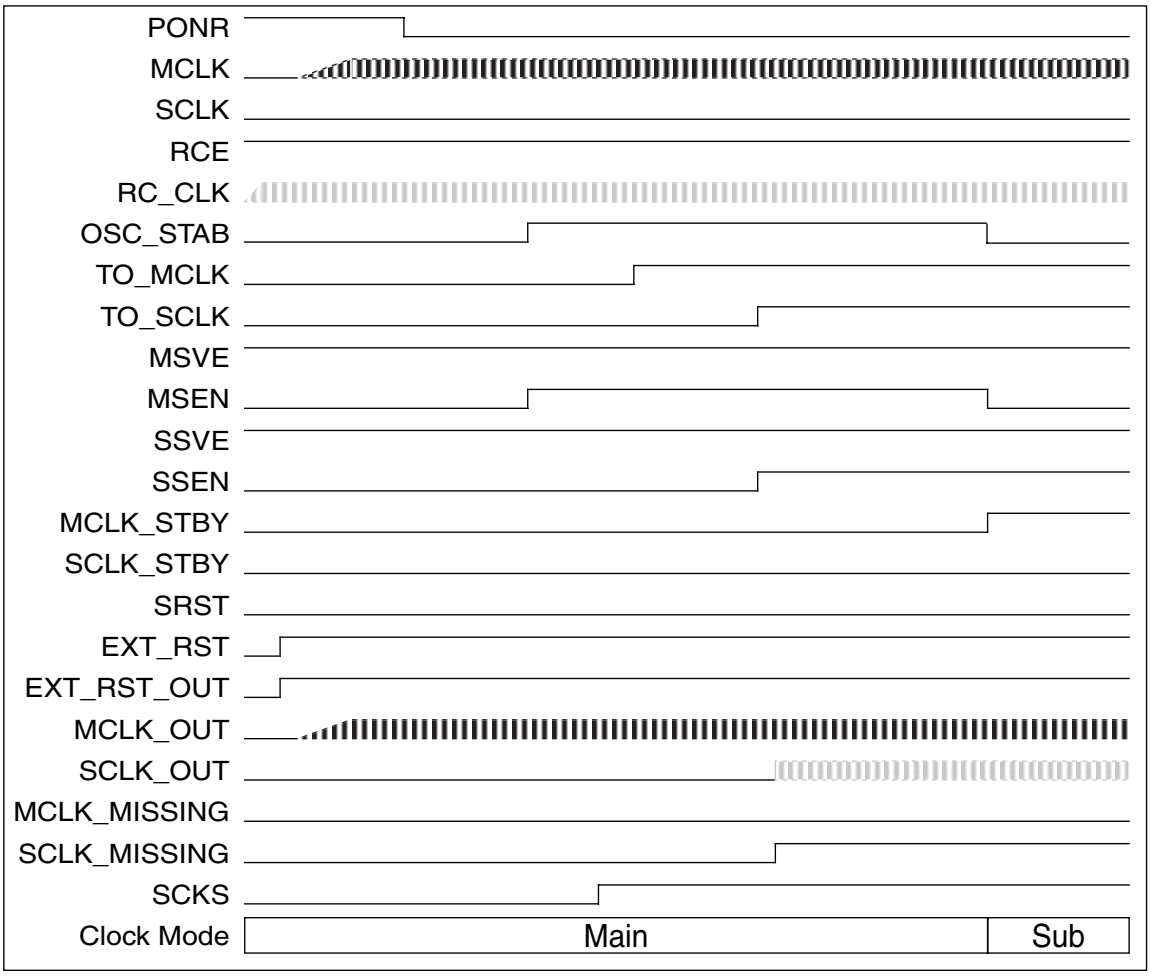
(Note) New feature: RCE setting is valid if HWWD.STPRUN (HWWD[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

- The RC-oscillator is enabled immediately after wake-up from STOP state.
- If the Main clock was disabled in STOP: The Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing after wake-up from STOP state, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- IF the Sub clock was disabled in STOP: The Sub clock supervisor is enabled after the ’Sub clock timeout’ (TO_SCLK) from the timeout counter which is clocked with the CLKRC.

■ RC-Clock as Sub Clock

The Sub clock supervisor can provide the CLKRC as Sub clock. To enable this feature, SCKS bit (bit7 of CSVCR) must be set to ’1’.

Figure 4-12 Timing Diagram: Sub clock mode with single clock device



■ Check if reset was asserted by the Clock Supervisor

To find out whether the Clock Supervisor has asserted reset, the software must check the reset cause by reading the RSRR register (See "RSRR: Reset Cause Register" on P. 141). On the most flash devices, the RSRR register is read and cleared by the Boot ROM software. The content of RSRR can be found in CPU register R4[7:0] after Boot ROM is done.
If INIT (bit 7 of RSRR) is set, the cause was either external reset at the INITX pin or the clock supervisor or the hardware watchdog (HWWD). If neither SM bit nor MM bit (bit 5 and bit 6 of CSVCR) is set, reset cause was the external reset or the hardware watchdog. If SM is ’1’ the reset cause is a missing Sub clock and if MM is ’1’ the reset cause is a missing Main clock.

5. Cautions

After a Clock Supervisor reset, the CLKPLL is not usable as clk source, if the clock supervisor reset was caused by a missing OSCMAIN.