Errata

This errata sheet is for MB91350A Series Hardware Manual Rev.3 (CM71-10121-3E)

FR60
32-BIT MICROCONTROLLER
MB91350A Series
HARDWARE MANUAL

2008.12.24

Date	Page	Item	Description
2008/ 12/24	36	2.1	The following description of "2.1 Precautions on Handling the Device" was added as indicated by the shading below. ■ Synchronous Mode Software Reset When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0". ・Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0) ・NMI not used
2008/ 6/18	48	3.1	"■ Memory Map" was corrected as indicated by the shading below. (Error) ・The available internal RAM area is restricted as soon as a reset is cleared. If the available area setting would be rewritten, include at least one NOP instruction immediately after that processing. (Correct) ・The available internal RAM area is restricted as soon as a reset is cleared. If the available area setting would be rewritten, include at least one NOP instruction immediately after that processing. For details, see CHAPTER 19 "DATA INTERNAL RAM/INSTRUCTION INTERNAL RAM ACCESS RESTRICTION FUNCTIONS". [mcu_doc0671]
2008/ 12/24	103	3.9.5	The following description of "■ Synchronous Reset Operation" was added as indicated by the shading below. Note: The restrictions that apply to bit9:SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.
2008/ 12/24	113	3.10.6	The following description of "[Bit 11] SRST (Software ReSeT occurred)" in "■ Reset Source Register/Watchdog Timer Control Register (RSRR)" was added as indicated by the shading below. [Bit 11] SRST (Software ReSeT occurred) This bit indicates whether a reset (RST) occurred due to writing to the SRST bit of the STCR register (a software reset). Note the restrictions that apply to bit9:SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.

Date	Page	Item	Description
2008/ 12/24	118	3.10.6	The following description of "[Bit 9] SYNCR (SYNChronous Reset enable)" in "■ Timebase Counter Control Register (TBCR)" was added as indicated by the shading below. Note: When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0". ・Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0) ・NMI not used

FUJITSU

Corrections of Hardware Manual

MB91350A

hm91350-cm71-10121-3e-corr-x1-00.doc

Addendum, MB91350 Hardware Manual (CM71-10121-3E)

This is the Addendum for the Hardware Manual CM71-10121-2E of the MB91350A microcontroller series. It describes all known discrepancies of the MB91350A microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM91350001	13.05.04	1.00	15	I²C INTERFACE, Note added
HWM91350002	09.12.04	1.00	16	DMAC overrun, Note added
HWM91350003	09.12.04	1.00	3	WDT and standby, Note added

HWM91350001 TOP

CHAPTER 15 I²C INTERFACE

Restriction of specification at sending General Call Address for MCU with I2C

When using Multi-Master mode for I2C and another Master is sending a General Code Address at same time as Fujitsu MCU, an arbitration lost* occurs after 2nd byte.
Under following conditions the restriction do not exist:
- No usage of I2C peripheral
- Usage of I2C with Single Master system
- Usage of I2C with Multi Master system, no General Call Address used
- Usage of I2C with Multi Master system, General Call Address used by Fujitsu MCU, only
- Usage of I2C with Multi Master system, General Call Address used. If the value of data, send by Fujitsu MCU, is smaller than another transfer data, the arbitration lost does not occur.

*: If the data value is smaller than another one, oneself never has "Arbitration lost" because one with large transmission data value will have "Arbitration lost".

HWM91350002 TOP

Chapter 16 DMA Controller (DMAC)

DMA transfer overrun

During DMA demand transfer, after DMA transfer request signal DREQ is cancelled within external bus cycle before rising Write strobe, an extra transfer is implemented, leading to a demand transfer overrun.

Several conditions for this overrun and workaround are described in application note “FR Family Product DMA Demand Transfer Overrun” in FR60_DMA_OverrunE.pdf.

HWM91350003 TOP

Chapter 3 CPU and Control Units

Watchdog Failure in Standby Mode

The Watchdog timer (WDT) reset normally occurs at the second falling edge of the timebase counter bit output in the specified WDT cycle.

However, there is special timing when changing to standby mode, which can lead to premature reset. If a wake-up interrupt occurs within two cycles after transition to standby mode and the timbase timer counter bit for WDT is currently 1, then WDT reset will occur at next falling edge of timebase timer counter bit. This will happen even if this is the first falling edge (instead of second one) after last WDT clear operation and can lead to an early reset.

To avoid early reset, it is recommended to clear timebase timer counter before transition to standby mode. This gives enough time to enter standby mode before timebase timer counter bit becomes 1.

The application note FR60_WDT_FaileE.pdf describes conditions and workaround.