

**Errata**

This errata sheet is for MB91301 Series Hardware Manual Rev.4 (CM71-10114-4E)

FR60  
32-BIT MICROCONTROLLER  
MB91301 Series  
HARDWARE MANUAL

2009.10.8

□ : Corrected part

Date	Page	Item	Description
2008/9/2	-	-	See the following page for details.
2008/12/19	36	2.1	<p>The following description of "○ MB91301 series" in "■ Precautions on Use" was added as indicated by the shading below.</p> <ul style="list-style-type: none"> <li>• Synchronous Mode Software Reset</li> </ul> <p>When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0".</p> <ul style="list-style-type: none"> <li>• Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0)</li> <li>• NMI not used</li> </ul>
2008/12/19	101	3.11.5	<p>The following description of "■ Synchronous Reset Operation" was added as indicated by the shading below.</p> <p>Note the restrictions that apply to bit 9: SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.</p>
2008/12/19	111	3.12.6	<p>The following description of " [bit11] SRST (Software ReSeT occurred) " in "■ Reset Source Register/Watchdog Timer Control Register (RSRR) " was added as indicated by the shading below.</p> <p>[bit11] SRST (Software ReSeT occurred) This bit indicates whether a reset (RST) occurred due to writing to the SRST bit of the STCR register (a software reset).</p> <p>Note the restrictions that apply to bit9:SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.</p>
2008/12/19	116	3.12.6	<p>The following description of " [bit9] SYNCR (SYNChronous Reset enable) " in "■ Time Base Counter Control Register (TBCR) " was added as indicated by the shading below.</p> <hr/> <p>Note:</p> <p>When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0".</p> <ul style="list-style-type: none"> <li>• Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0)</li> <li>• NMI not used</li> </ul> <hr/>

Date	Page	Item	Description
2009/10/8	313	8.3	<p>“○ Asynchronous (start-stop synchronization) mode” in “■ Calculation of Baud Rate” was deleted as indicated by the shading below.</p> <p>Maximum bps 34MHz 531250 bps, 68MHz 1062500 bps</p>
2009/10/8	313	8.3	<p>“○ CLK synchronous mode” in “■ Calculation of Baud Rate” was deleted as indicated by the shading below.</p> <p>Maximum bps 34MHz 8500000 bps, 68MHz 17000000 bps</p>
2009/10/8	349	12.2.1	<p>“Note” in “■ Detailed Bit of Control Status Register(ADCS)” was added indicated by the shading below.</p> <p>Note :</p> <p>In the case of immediately reading the state after starting the A/D conversion, there is the delay of several cycles in the changing from "BUSY bit" to "1", and it might be read "0" which is the state before the A/D conversion starting. Therefore, we recommend to use "INT bit" for judging the end of A/D conversion.</p>
2009/10/8	350	12.2.1	<p>“Note” in “[bit12]CRF (Convert Run Flag): A/D converting status” was deleted as indicated by the shading below.</p> <p>Note :</p> <p>Do not change analog input value during A/D converting.</p>



## Corrections of Hardware Manual

# MB91301

hm90301-cm71-10114-4e-corr-x1-00

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### Addendum, MB91301 Hardware Manual (CM71-10114-4E)

This is the Addendum for the Hardware Manual CM71-10114-4E of the MB91301 microcontroller series. It describes all known discrepancies of the MB91301 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
<a href="#">HWM91301001</a>	12.05.04	1.00	16	I <sup>2</sup> C INTERFACE, Note added
<a href="#">HWM91301002</a>	09.12.04	1.00	14	DMAC overrun, Note added
<a href="#">HWM91301003</a>	09.12.04	1.00	3	WDT and standby, Note added

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## Chapter 16 I<sup>2</sup>C INTERFACE

Restriction of specification at sending General Call Address for MCU with I2C

When using Multi-Master mode for I2C and another Master is sending a General Code Address at same time as Fujitsu MCU, an arbitration lost\* occurs after 2nd byte.

Under following conditions the restriction do not exist:

- No usage of I2C peripheral
- Usage of I2C with Single Master system
- Usage of I2C with Multi Master system, no General Call Address used
- Usage of I2C with Multi Master system, General Call Address used by Fujitsu MCU, only
- Usage of I2C with Multi Master system, General Call Address used. If the value of data, send by Fujitsu MCU, is smaller than another transfer data, the arbitration lost does not occur.

\*: If the data value is smaller than another one, oneself never has "Arbitration lost" because one with large transmission data value will have "Arbitration lost".

## Chapter 14 DMA Controller (DMAC)

DMA transfer overrun

During DMA demand transfer, after DMA transfer request signal DREQ is cancelled within external bus cycle before rising Write strobe, an extra transfer is implemented, leading to a demand transfer overrun.

Several conditions for this overrun and workaround are described in application note "FR Family Product DMA Demand Transfer Overrun" in FR60\_DMA\_OverrunE.pdf.

## Chapter 3 CPU and Control Units

Watchdog Failure in Standby Mode

The Watchdog timer (WDT) reset normally occurs at the second falling edge of the timebase counter bit output in the specified WDT cycle.

However, there is special timing when changing to standby mode, which can lead to premature reset. If a wake-up interrupt occurs within two cycles after transition to standby mode and the timebase timer counter bit for WDT is currently 1, then WDT reset will occur at next falling edge of timebase timer counter bit. This will happen even if this is the first falling edge (instead of second one) after last WDT clear operation and can lead to an early reset.

To avoid early reset, it is recommended to clear timebase timer counter before transition to standby mode. This gives enough time to enter standby mode before timebase timer counter bit becomes 1.

The application note FR60\_WDT\_FaileE.pdf describes conditions and workaround.