

Errata

This errata sheet is for MB91270 Series Hardware Manual Rev.2 (CM71-10128-2E)

FR60Lite
 32-BIT MICROCONTROLLER
 MB91270 Series
 HARDWARE MANUAL

2009.5.12

Date	Page	Item	Description
2009/ 3/9	-	-	MB91F278(S) was deleted.
2008/ 9/16	4	1.1	<p>■ I/O Port was corrected as indicated by the shading below.</p> <ul style="list-style-type: none"> • Maximum 128 ports → Maximum 128 ports(MB91V280)/ Maximum 82 ports(MB91F273(S)/F278(S))
2009/ 3/3	32	2.1	<p>The following description in “2.1 Precautions when Handling Devices” was added.</p> <p>■ Serial Communication</p> <p>There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.</p> <p style="text-align: right;">[mcu_doc0960]</p>
2008/ 6/13	342	11.5.1	<p>"■ Message Object" was corrected as indicated by the shading below.</p> <p>(Error) The message object settings for the message RAM (except the MsgVal, NewDat, IntPnd, and TxRqst bits) are not initialized by the resetting of hardware. Therefore, initialize message objects by the CPU or set the MsgVal bit to invalid (MsgVal=0). Also, set the CAN bit timing register when the Init bit in the CAN control register is "0".</p> <p>(Correct) The message object settings for the message RAM (except the MsgVal, NewDat, IntPnd, and TxRqst bits) are not initialized by the resetting of hardware. Therefore, initialize message objects by the CPU or set the MsgVal bit to invalid (MsgVal=0). Also, set the CAN bit timing register (BTR) and BRP Extension Register(BRPER) when the Init bit in the CAN control register is "1" and CCE bit is "1".</p> <p style="text-align: right;">[mcu_doc:0735]</p>

Date	Page	Item	Description										
2008/9/16	375	12.3.1	<p>The following description of "[bit10] CRE: Receive error flag clear bit" in "■ Serial Control Register (SCR)" was added as indicated by the shading below.</p> <p>[bit10] CRE: Receive error flag clear bit</p> <table border="1"> <thead> <tr> <th rowspan="2">CRE</th> <th colspan="2">Reception error clear</th> </tr> <tr> <th>Write</th> <th>Read</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No effect [Initial value]</td> <td rowspan="2">Read value is always "0"</td> </tr> <tr> <td>1</td> <td>Clear all reception errors (PE, FRE, ORE).</td> </tr> </tbody> </table> <p>This bit clears PE, FRE, and ORE flags of serial status register (SSR). This bit also clears reception error interrupt factors. Writing "1" clears the error flag. Writing "0" is no effect. Reading always returns "0".</p> <hr/> <p>Note: Clear the reception error flag after disabling reception (RXE=0). When the reception error flag is cleared without disabling the reception, the reception is interrupted once at that timing and then it restarts. Therefore, when the reception is restarted, incorrect data might be received.</p> <hr/> <p style="text-align: right;">[mcu_doc:0806]</p>	CRE	Reception error clear		Write	Read	0	No effect [Initial value]	Read value is always "0"	1	Clear all reception errors (PE, FRE, ORE).
CRE	Reception error clear												
	Write	Read											
0	No effect [Initial value]	Read value is always "0"											
1	Clear all reception errors (PE, FRE, ORE).												
2009/3/3	393	12.4	<p>The following description of "Note:" in "■ Reception Interrupt" was corrected as indicated by the shading below.</p> <p>(Error) Note: CRE bit is write only. When writing "1", "1" is retained for 1 machine cycle.</p> <p>(Correct) Note: Disable reception (RXE=0) and then clear reception error flags in CRE bit. If the reception error flag is cleared without disabling reception, the reception is interrupted once and then the reception is resumed. By this operation, some data may not be received normally at the resume.</p> <hr/> <p style="text-align: right;">[mcu_doc0960]</p>										
2008/6/13	407	12.6	<p>"■ Operation Enable Bit" was corrected as indicated by the shading below.</p> <p>(Error)</p> <ul style="list-style-type: none"> If reception operation is disabled during reception (data is inputted to the reception shift register), finish frame reception and read the received data of the reception data register (RDR), and then stop the reception operation. If the transmission operation is disabled during transmission (data is outputted from the transmission shift register), wait until there is no data in the transmission data register (TDR) before stopping the transmission operation. <p>(Correct)</p> <ul style="list-style-type: none"> If reception operation is disabled during reception (data is inputted to the reception shift register), stops the reception operation immediately. If the transmission operation is disabled during transmission (data is outputted from the transmission shift register), stops the transmission operation immediately. <hr/> <p style="text-align: right;">[mcu_doc0750]</p>										
2009/3/3	429	12.7	<p>Reference 1 was added in "12.7 Precautions when Using UART".</p> <hr/> <p style="text-align: right;">[mcu_doc0960]</p>										

Date	Page	Item	Description
2009/ 3/3	539	19.3	The following description was deleted from the "■ Interrupt Generation Timing". <ul style="list-style-type: none"> When interrupt is generated, count is stopped until clearing interrupt flag. <p style="text-align: right;">[mcu_doc0946]</p>
2008/ 9/16	612	26.2.2	■ Bit Configuration of Wait Register was corrected as indicated by the shading below. [bit5,bit4] "Use it by the default configuration usually" is added.
2008/ 9/16	629	26.5.2	Figure 26.5-1 Example of Write Procedure (in Flash Memory) was corrected as indicated by the shading below. Enable writing to FLASH memory with WE (bit 5) in FLCR. → Enable writing to FLASH memory with WE (bit 1) in FLCR. Disable writing to FLASH memory with WE (bit 5) in FLCR. → Disable writing to FLASH memory with WE (bit 1) in FLCR.
2008/ 9/16	632	26.5.3	Figure 26.5-2 Example of the Sector Erase Procedure was corrected as indicated by the shading below. Enable erasure in FLASH memory with WE (bit 5) in FLCR. → Enable erasure in FLASH memory with WE (bit 1) in FLCR. Disable erasure in FLASH memory with WE (bit 5) in FLCR. → Disable erasure in FLASH memory with WE (bit 1) in FLCR.

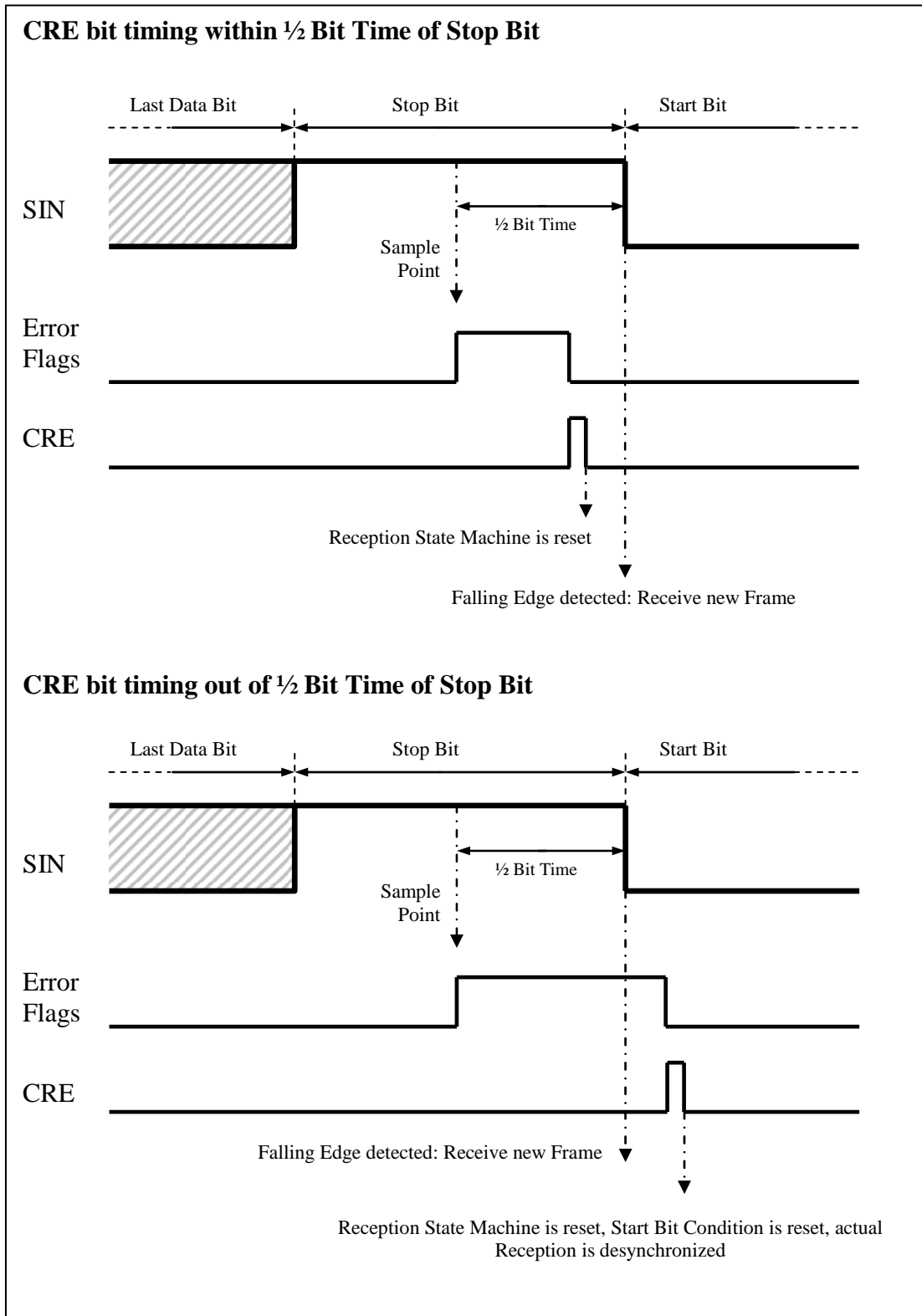
● Handling framing errors

- 1) (Graphic 1) CRE resets reception state machine and next falling edge at SINn starts reception of new byte (graphic 1).

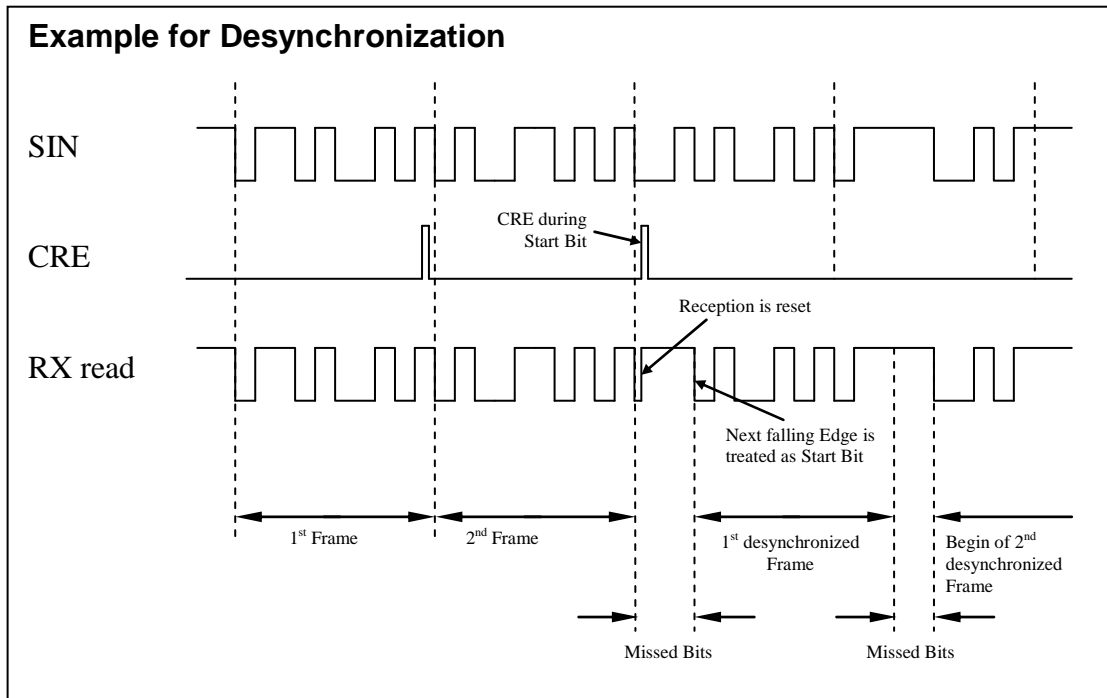
Therefore either set CRE bit immediately (within half bit time) after receiving errors to prevent data stream desynchronization (Graphic 2) or wait an application dependent time after receiving errors and set CRE, when SINn is idle.

- 2) Please note, that in case a framing error occurred (stop bit: SINn = "0") and next start bit (SINn = "0") follows immediately, this start bit is recognized regardless of no falling edge before (Graphic 3). This is used to remain UART synchronized to the data stream and to detect that serial data input (SINn) keeps "L" level (Graphic 3 above) by producing next framing errors. If this behavior is not wanted, please disable the reception temporarily RXE = 1 -> 0 -> 1 after framing error. In this case, reception goes on at next falling edge on SINn. (Graphic 3 below).

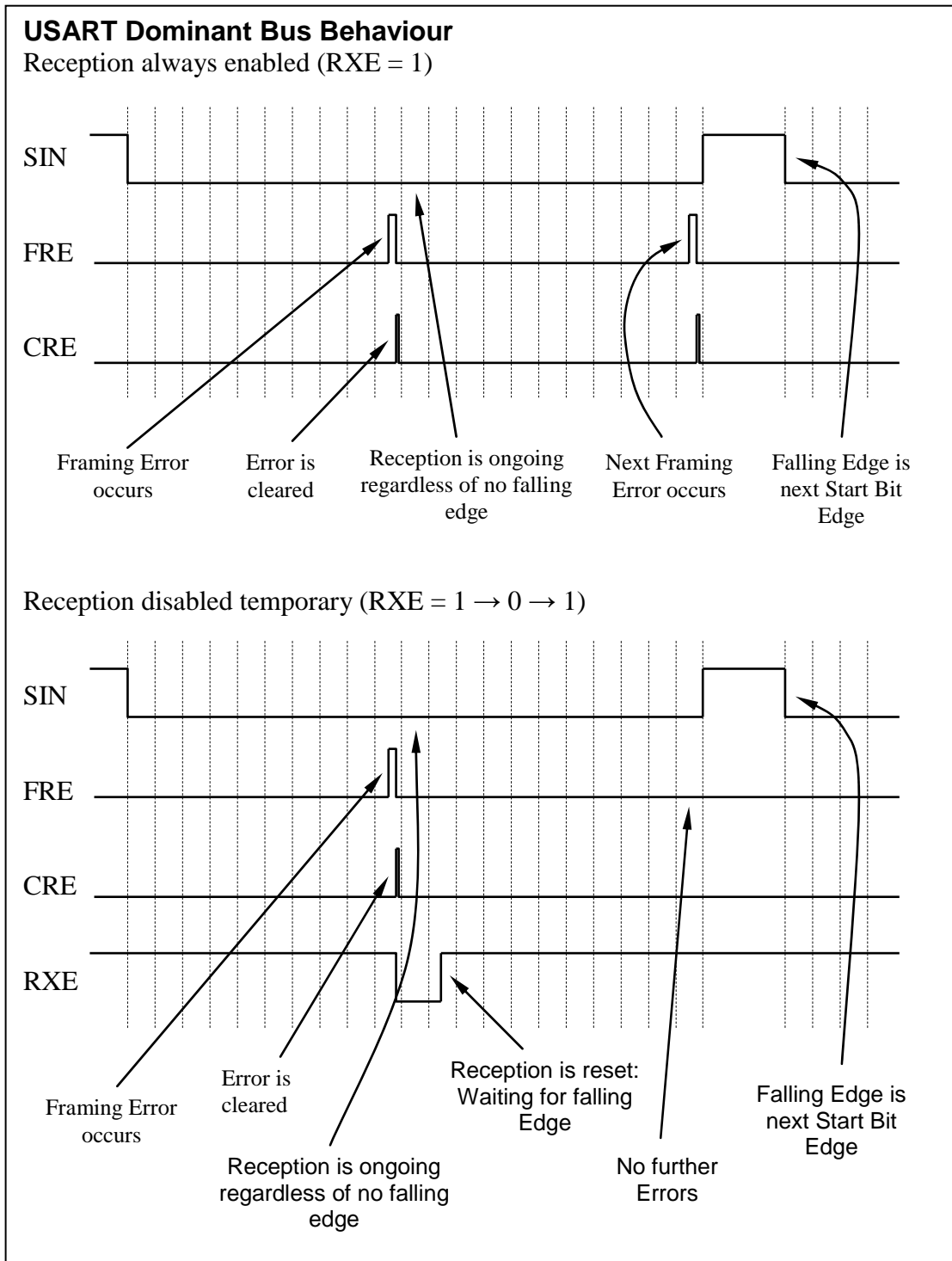
Graphic 1:



Graphic 2:



Graphic 3:





Corrections of Hardware Manual

MB91270

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Addendum, MB91270 Hardware Manual (CM71-10128-2E)

This is the Addendum for the Hardware Manual CM71-10128-2E of the MB91270 microcontroller Series. It describes all known discrepancies of the MB91270 microcontroller Series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd. mm. yy	Version No.	Chapter/Page	Description/Correction
HWM91270001	19. 04. 06	1. 02	12. 6. 2	Operation in Synchronous Mode, Typo corrected, Communication flow changed.

Chapter 12.6.2 - Operation in Synchronous Mode (Operation Mode 2)

For initialization of the synchronous **slave** mode, following settings have to be done.

Corrected flow
=====

Communication:

For initialization of the synchronous slave mode, following settings have to be done:

Baud rate generator registers (BGR):

Setting of reload value to dedicated baud rate reload counter.

Serial control register (SCR):

RXE, TXE: set both of these flags to "0"

SBL, AD: No stop bit. No address/data delimiter. The value is invalid.

CL: Fixed to 8-bit automatically. The value is invalid.

CRE: '1' (Error flag is cleared to initialize and transmission/reception are stopped.)

SSM='0': No parity. Setting value of PEN and P are invalid.

SSM='1': Setting of PEN and P are valid.

Serial mode control register (SMR):

MD1, MD0: "10B" (Mode 2)

SCKE: "1" (using of dedicated baud rate reload counter)

"0" (external clock input)

Serial status register (SSR):

BDS: "0" (LSB first) , '1' (MSB first)

RIE: "1" (interrupt enabled) , '0' (interrupt disabled)

TIE: "1" (interrupt enabled) , '0' (interrupt disabled)

Extended communication control register (ECCR):

SSM: '0' (without start/stop, normal)

'1' (with start/stop, special)

MS: '0' (master mode, UART generates serial clock.)

'1' (slave mode, UART receives serial clock from external.)

Serial control register (SCR):

RXE, TXE: set one or both of these control bits to "1" to begin communication.

Write the data to transmission data register (TDR) to start the communication.
For reception, stop output in
serial output enable (SOE) bit of SMR and then write the dummy data to TDR

(MWi)