

Errata

This errata sheet is for MB91265A Series Hardware Manual Rev.4 (CM44-10130-4E)

FR60Lite
32-BIT MICROCONTROLLER
MB91265A Series
HARDWARE MANUAL

2009.4.1

Date	Page	Item	Description												
2009/4/1	360	15.4.2.2	<p>The following description of "[bit2] TxRqst/NewDat: Message transfer request bit" in "■ Function of Registers" was corrected as indicated by the shading below.</p> <p>(Error)</p> <table border="1"> <thead> <tr> <th>TxRqst/NewDat</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Indicates that "0" is set to the TxRqst bit of the message object * and CAN transmission request register. [Initial value]</td> </tr> <tr> <td style="text-align: center;">1</td> <td>"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th>TxRqst/NewDat</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td>Indicates that the TxRqst bit of CAN transmission request register and the message object * are not to be changed. [Initial value]</td> </tr> <tr> <td style="text-align: center;">1</td> <td>"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).</td> </tr> </tbody> </table> <p style="text-align: right;">[mcu_doc:0889]</p>	TxRqst/NewDat	Function	0	Indicates that "0" is set to the TxRqst bit of the message object * and CAN transmission request register. [Initial value]	1	"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).	TxRqst/NewDat	Function	0	Indicates that the TxRqst bit of CAN transmission request register and the message object * are not to be changed. [Initial value]	1	"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).
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2008/6/13	381	15.4.4.3	<p>■ Function" of Registers was added as indicated by the shading below.</p> <ul style="list-style-type: none"> Set condition - When WR/RD of IFx command mask register is set to "1" and IntPnd of IFx message control register is set to "1", IntPnd of specific object can be set by writing to IFx command request register. 												
2008/6/13	381	15.4.4.3	<p>■ Function" of Registers was corrected as indicated by the shading below.</p> <ul style="list-style-type: none"> Reset condition <p>(Error)</p> <p>When IFx command mask register sets WR/RD and ClrIntPnd to "1",</p> <p>(Correct)</p> <p>When IFx command mask register sets WR/RD and CIP to "1",</p>												
2008/6/13	381	15.4.4.3	<p>■ Function" of Registers was added as indicated by the shading below.</p> <ul style="list-style-type: none"> Reset condition - When WR/RD of IFx command mask register is set to "1" and IntPnd of IFx messagecontrol register is set to "0", IntPnd of specific object can be reset by writing to IFx command request register. 												

Date	Page	Item	Description
2008/ 6/13	386	15.5.1	<p data-bbox="443 289 1081 315">"■ Message Object" was corrected as indicated by the shading below.</p> <p data-bbox="443 346 509 371">(Error)</p> <p data-bbox="443 375 1482 457">Message object setting of message RAM (except for MsgVal, NewDat, IntPnd and TxRqst bits) is not initialized by hardware reset. So, initialize the message object by CPU or set the MsgVal bit invalid (MsgVal=0). Set the CAN bit timing register also when Init bit of CAN control register is "0".</p> <p data-bbox="443 485 526 510">(Correct)</p> <p data-bbox="443 514 1482 621">Message object setting of message RAM (except for MsgVal, NewDat, IntPnd and TxRqst bits) is not initialized by hardware reset. So, initialize the message object by CPU or set the MsgVal bit invalid (MsgVal=0). Set the CAN bit timing register(BTR) and CAN prescaler extension register (BRPER) also when Init bit of CAN control register is "1" and CCE bit is "1".</p> <p data-bbox="1325 648 1482 674" style="text-align: right;">[mcu_doc:0735]</p>



Corrections of Hardware Manual

MB91265

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Addendum, MB91265 Hardware Manual (CM71-10130-4E)

This is the Addendum for the Hardware Manual CM71-10130-4E of the MB91265 microcontroller series. It describes all known discrepancies of the MB91265 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM91265001	02.05.06	1.00	12.4.9/240	Typo in the table for input capture control register (ch2, ch3), lower byte (ICSL23)

There is a typo in the table for input capture control register (ch2, ch3), lower byte (ICSL23). The correction is marked grey in the following table.

The bit-name of bit 6 (ICSL23) is ICP2 instead of IP2.

■ Input Capture State Control Register (ch2, ch3), Lower Byte (ICSL23)

