

## Errata

This errata sheet is for MB91260B Series Hardware Manual Rev.2 (CM71-10127-2E)

FR60Lite  
32-BIT MICROCONTROLLER  
MB91260B Series  
HARDWARE MANUAL

2009.4.1

Date	Page	Item	Description
2009/ 4/1	24	2.1	<p>The following description of "■ Handing Devices" was added as indicated by the shading below.</p> <p>● Synchronous Mode Software Reset</p> <p>When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0".</p> <ul style="list-style-type: none"> <li>• Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0)</li> <li>• NMI not used</li> </ul>
2009/ 4/1	71	3.11.1	<p>"● Setting of PLL multiplier" was deleted as indicated by the shading below.</p> <p>● Setting of PLL multiplier</p> <p>To change the PLL multiplier setting from the initial value, start program operation and set the new value either before or at the same time as enabling the PLL for oscillation. After changing the multiplier, switch the source clock after the lock wait time has passed. For this PLL lock wait time, it is recommended to use a timebase timer interrupt.</p> <p>Before changing the PLL multiplier setting during operation, switch the source clock to any resource other than the PLL. After changing the multiplier, switch the source clock after the lock wait time has passed in the same way as above.</p> <p>The PLL multiplier setting can be changed while the PLL is being used. In this case, however, the device enters the oscillation stabilization wait state automatically after updating the PLL multiplier and stops program operation until the oscillation stabilization wait time has passed. When the clock source is switched to any resource other than the PLL, the device does not stop program operation.</p> <p style="text-align: right;">[mcu_doc:0849]</p>
2009/ 4/1	78	3.11.6	<p>The following description of "[bit11] SRST (Software ReSeT occurred)" in "■ RSRR: Reset Source Register/watchdog Timer Control Register" was added as indicated by the shading below.</p> <p>[bit11] SRST (Software ReSeT occurred)</p> <p>This bit indicates whether a reset (RST) by writing to the SRST bit (software reset) in the STCR register has occurred.</p> <p>Note the restrictions that apply to bit9:SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.</p>
2009/ 4/1	82	3.11.6	<p>The following description of "[bit9] SYNCR (SYNChronous Reset enable)" in "■ TBCR: Timebase Counter Control Register" was added as indicated by the shading below.</p> <hr/> <p>Note:</p> <p>When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0".</p> <ul style="list-style-type: none"> <li>• Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0)</li> <li>• NMI not used</li> </ul> <hr/>