



Corrections of Hardware Manual

MB91109

Hm9 109-cm71-10106-1e-corr-x1-01

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Addendum, MB91109 Hardware Manual (CM71-10106-1E)

This is the Addendum for the Hardware Manual CM71-10106-1E of the MB91109 microcontroller series. It describes all known discrepancies of the MB91109 microcontroller series Hardware Manual.

| Ref. Number (Text Link) | Date dd.mm.yy | Version No. | Chapter/Page | Description/Correction |
|-----------------------------|------------------|----------------|--------------|---|
| HWM91109001 | 28.06.00 | V1.00 | 16.5 | Flash Memory Access, with 2 cycles at 25MHz |
| HWM91109002 | 09.10.02 | V1.01 | 15 | DMA Transfer Request Causes added |
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HWM91109001

Chapter 16.5 Flash Memory Access Mode

FLASH on C-Bus can be accessed with 2 cycles of 25MHz clock. The bus width is 32bit and if instructions are sequentially fetched, each 16bit instruction can be executed at one 25MHz clock.

HWM91109002

Chapter 15 DMAC

DMA Transfer Request Causes are not included in the Manual.

See table below:

| Channel number | Transfer request cause |
|-----------------------|---|
| 0 | External transfer request input pin DREQ0 |
| 1 | External transfer request input pin DREQ1 |
| 2 | External transfer request input pin DREQ2 |
| 3 | PWM ch0 |
| 4 | UART ch0 received |
| 5 | UART ch0 sent |
| 6 | 16-bit reload timer ch0 |
| 7 | A/D converter |