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Fujitsu Microelectronics Europe
Functional Limitation Report

32-BIT MICROCONTROLLER

MB91460 SERIES

MB91V460

FUNCTIONAL LIMITATION
DMA FLASH INTERFACE ARBITRATION

2008-10-06

FUJITSU

Revision History

Date	Issue
2008-10-06	V1.0, initial version

This document contains 9 pages.

Abbreviations:

FME	Fujitsu Microelectronics Europe GmbH
MCU	Microcontroller

Contents

Fujitsu does not bear any warranty in the case this handling note is not fully observed.

1 Problem Description

A problem was found in the flash interface arbitration logic on the evaluation device MB91V460A of the MB91460 series.

The problem does not occur if the flash instruction cache is disabled or if the number of wait cycles for flash memory access (FMWT_WTC) is below or equal to two.

Under certain conditions a flash code access may get corrupted, resulting in executing wrong instruction code and/or a wrong entry into the flash instruction cache. This problem is called ‘DMA flash interface arbitration problem’.

The pre-fetch function is not affected by this problem.

Affected part numbers are listed below.

2 Problem Conditions

The problem may occur if the following conditions are all met simultaneously:

- The flash instruction cache is enabled.
- The number of wait cycles for flash memory access (FMWT_WTC) is > 2.
- There is a flash instruction cache miss.
- After that, there are two flash instruction cache hits and in parallel an F-bus data access from DMA to the flash, which then causes the problem.

3 Affected Devices

The following devices were affected:

- MB91V460RB-ES

4 Affected Modules

This problem is affecting the flash interface equipped with:

- Flash Instruction Cache

The pre-fetch function is not affected by this problem.

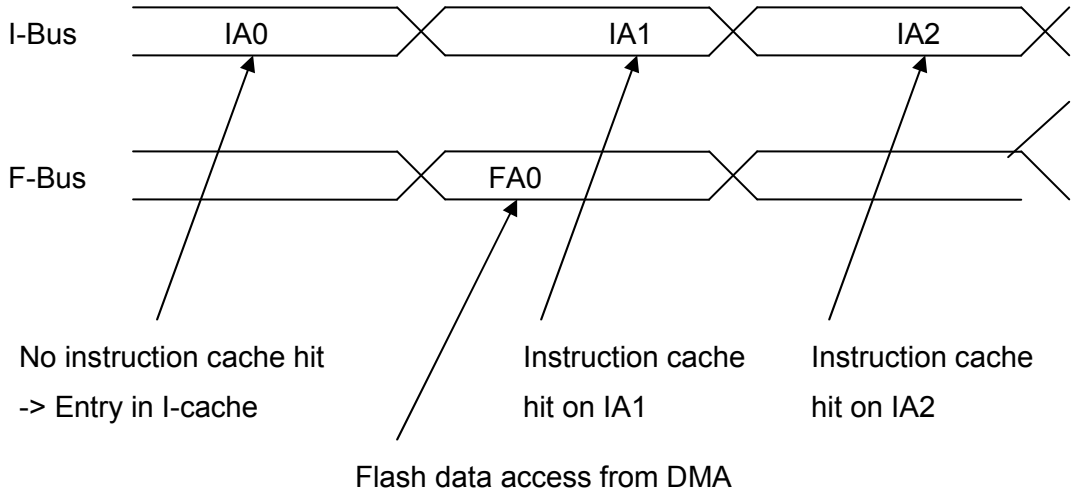
5 DMA data access to Flash Memory area

The problem occurs in the following constellation:

- The flash instruction cache has to be enabled.
- Number of wait cycles for flash memory access (FMWT_WTC) > 2.
- There is a flash instruction cache miss.
- After that, there are two flash instruction cache hits and in parallel an F-bus data access from DMA to the Flash, which causes the problem.

In the case that the CPU is doing a read operation to the Flash memory the code execution is stalled until the data is captured in the CPU. Therefore no subsequent instruction cache hit to the first instruction hit can occur. There is no problem.

In contrast when using the DMA to transfer data from Flash memory: in that case due to continuous program operation a subsequent instruction cache hit can occur after the first instruction hit. Here the problem can occur depending on exact timing of instruction hits and DMA access.



- CLKB Cycle 1: Instruction #IA0 output from flash -> write to I-Cache
- CLKB Cycle 2: I-Cache RAM read-after-write wait cycle
  F-bus data access from DMA to Flash in parallel,
  causing the problem.
- CLKB Cycle 3: I-cache hit on instruction #IA1
- CLKB Cycle 4: I-cache hit on instruction #IA2
- CLKB Cycle n: Wrong output of instruction #IA3 to I-Bus and/or entry to I-Cache

Code execution on MB91V460A using emulation SRAM is affected by this problem due to the significant shortening of the access time to the emulation SRAM. Abnormal program execution may occur.

In case of disabled flash instruction cache or if the number of wait cycles for flash memory access is below or equal to two, the problem does not occur. The selected wait cycles for flash memory limits the maximum core frequency. Please check the hardware manual, too.

6 Workaround

6.1 Do not use DMA for data transfers from Flash memory

Not using the DMA for data transfers from Flash Memory will avoid the problem as described in chapter 5.

CPU data access to Flash Memory does not cause a problem on MB91V460A.

Remark: The pre-fetch function is not affected by this problem.

6.2 Transfer DMA data from Flash into (hidden) RAM of MB91V460A

DMA data transfer from D-RAM or ID-RAM does not cause the problem. Due to this fact, a possible workaround for using the emulator could be to transfer any relevant data in Flash memory into the additional (hidden) RAM areas of the MB91V460A device and to patch the DMA source addresses in the application code. This can be done via procedure file after downloading the application and avoids recompilation of the application.

Fujitsu can provide help on generating such a procedure file for user applications.

7 Corrective action by Fujitsu

Fujitsu has corrected this problem by a redesign of the flash instruction cache arbitration logic.

New part numbers and redesigns are scheduled as follows:

- MB91FV460B will be available from Jan/2009 on