

32-BIT MICROCONTROLLER  
**MB91F464A/MB91F465K**

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FUNCTIONAL LIMITATION  
CLOCK MODULATOR

2009-07-07



## Revision History

Date	Issue
2009-07-07	V1.0, Initial Version

This document contains 10 pages.

### Abbreviations:

FME            Fujitsu Microelectronics Europe GmbH  
MCU            Microcontroller

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**Fujitsu does not bear any warranty in the case this handling note is not fully observed.**

## 1 Problem Description

A malfunction of the clock modulator was found on MB91F464A and MB91F465K while improving the test set. The clock modulator does not output any clock in a certain frequency range (within specified input frequency range).

The clock modulator is outputting valid clocks above or below that frequency range. The effect is called “dead band of the clock modulator” due to its shape.

## 2 Problem Conditions

Problem may occur if all of the following conditions are met:

- Clock Modulator is enabled
- Clock modulator input frequency ( $F_{in}$ ) is  $> 48\text{MHz}$

### 2.1 Impact on application

If the CPU is running on PLL and clock modulation is enabled in the critical input frequency range then internal clocks which are based on PLL output are immediately stopped. Hence all modules based on PLL output (like CPU, DMA, Software-Watchdog) will be stopped.

Modules which use RC oscillation (e.g. Hardware-Watchdog, Clock-Supervisor) and modules which use main/sub oscillation (like RTC) are not stopped.

Since the CPU can not longer refresh the Hardware-Watchdog a reset will be issued after the watchdog time has elapsed, and application is restarting from reset.

## 3 Affected Devices

The following devices are affected:

- MB91F464AA (all date codes)
- MB91F464AB (all date codes)
- MB91F465KA (all date codes)
- MB91F465KB (all date codes)

## 4 Affected Modules

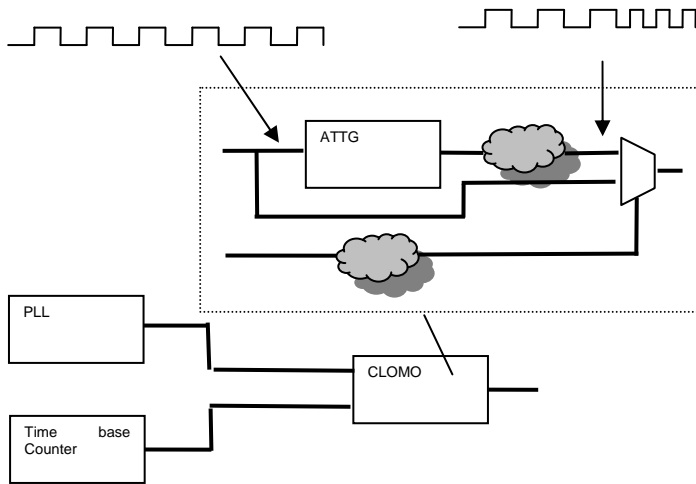
The following macros are affected:

- Clock Modulator

## 5 Root Cause

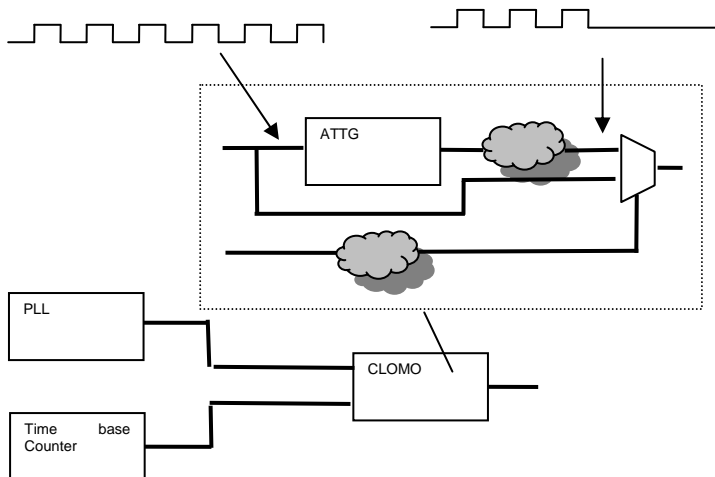
### 5.1 Startup behaviour

#### Startup behavior of the clock modulator outside dead band frequency



The clock modulator is switching the output clock from non-modulated clock to modulated clock. This is the correct and expected operation.

#### Startup behavior of the clock modulator within dead band frequency



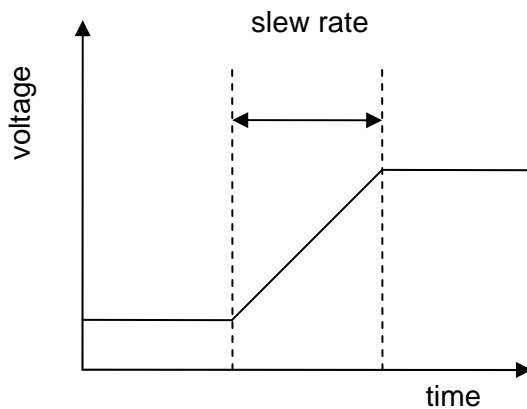
The clock modulator is NOT switching the output clock from non-modulated clock to modulated clock.



### 5.3 Identified problem

A timing analysis on the clock input of the clock modulator showed a slew rate of more than 1200 ps. A comparison with devices without the dead band effect showed a much smaller slew rate at smaller than 500ps.

It is proven that the increased slew rate is causing jitter in the ATTG/DLL part of the clock modulator which leads to an instable calibration causing an invalid signal transition when switching between non-modulated and modulated clock.



## 6 Workaround

### 6.1 Frequency setting

The behaviour of the clock modulator dead band is depending on input frequency. Using frequencies up to a specified limit will enable the clock modulator to work correctly.

Frequency settings:

- **$F_{in} \leq 48\text{MHz}$  : possible to use as input frequency to clock modulation**
- **$F_{in} > 48\text{MHz}$  : do not use as input frequency to clock modulation**

## 7 Corrective action by Fujitsu

- The library of the clock modulator is improved. A check of the signal slew rate driving the clock input will be added to prevent that problem in future devices.
- The data sheet of affected devices will be corrected to show 48 MHz maximum input frequency to clock modulation