

16/32-BIT MICROCONTROLLER
MB9FXXX

HANDLING NOTE
DATA POLLING FLAG DURING FLASH
SECTOR ERASE

2009-05-25



Revision History

Date	Issue
2009-05-25	V1.0, Initial Version

This document contains 11 pages.

Abbreviations:

CPU	Central Processing Unit
FME	Fujitsu Microelectronics Europe GmbH
MCU	Microcontroller

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Fujitsu does not bear any warranty in the case this handling note is not fully observed.

1 Introduction

This handling note offers clarification on handling of 'Flash sector erase' algorithm in certain microcontroller products. The documentation of affected products may be interpreted such that non-recommended implementation of 'Flash sector erase' operation can be applied.

Please note that in case a non-recommended procedure is in use, incorrect execution of 'Flash sector erase' algorithm is experienced immediately with high probability in the design phase of a product.

Programming tools supplied by Fujitsu are not affected.

2 Description

The built-in flash memory of Fujitsu microcontrollers has an automatic algorithm for the flash memory program/erase operation. When using the automatic algorithm, the status of each operation can be judged with the hardware sequence flags DQ7, DQ6, DQ5, DQ3, and DQ2.

The behaviour of one of these flags, the data polling flag DQ7, differs in one specific case between Fujitsu microcontrollers (16bit and 32bit) in 0.18µm technology and devices in preceding technologies (0.35µm/0.5µm). This difference is not described correctly in all Fujitsu hardware manuals.

This DQ7 flag behaves differently only during sector erase, when the flash is in the “sector erase wait state”. The sector erase completion might be misjudged by this behaviour if only the DQ7 flag is used to identify the termination of the sector erase operation.

Fujitsu PC serial programmer and parallel programmer also use a correct algorithm.

2.1 Sector erase procedure - behaviour of data polling flag DQ7

The data polling flag (DQ7) indicates if the automatic algorithm (write or erase) is being executed or has terminated. During a chip or sector erase (when the automatic algorithm is running), polling the DQ7 flag returns ‘0’. After completion of an erase operation, a read access to the Flash returns ‘1’ (content of erased Flash).

After submitting a sector erase command (writing of the last command ‘30H’), the Flash enters the ‘sector erase wait’ state for 40-160µs, what is indicated by DQ3=0. During this time the Flash waits for further erase commands (to erase multiple sectors at one time). The actual erase operation is started after this time (when DQ3 changes to ‘1’).

During this ‘sector erase wait’ state, the data polling flag DQ7 outputs ‘1’ in affected MCUs. DQ7 changes to “0” with entering the actual erase state.

For other MCUs, this behaviour is different: DQ7 outputs ‘0’ already in ‘sector erase wait’ state.

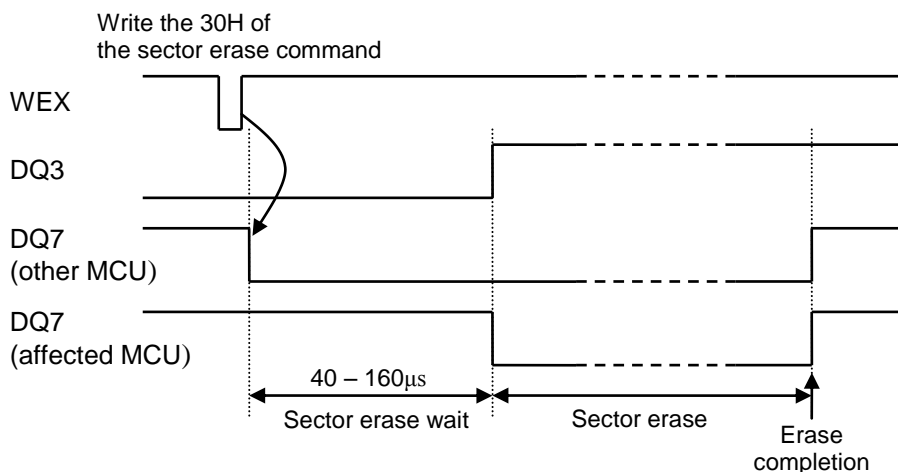


Figure 1: Operation of DQ7 and DQ3

This behaviour of the DQ7 flag is not described correctly or precisely in all hardware manuals. If the software only polls the DQ7 flag to detect the ‘erase completion’, then the software could misinterpret the ‘sector erase wait’ state as ‘erase completion’ in affected MCUs, although such software works correctly in other MCUs.

As a result, the CPU may start fetching instruction/data from flash during 'sector erase' and may misinterpret the hardware sequence flags as instruction/data, causing abnormal operation. Or the CPU tries to submit a second command which is not accepted by the flash or which accidentally puts the flash into 'sector erase suspend' state.

3 Problem Conditions

A problem may occur when the software tries to identify the 'sector erase' termination only by polling the DQ7 flag and if this polling is started within the 'sector erase wait' period of maximum 160µs after issuing the erase command.

4 Affected Devices

16/32bit	Product Series	Product name
16 bit	MB90880 series	MB90F882, MB90F882S, MB90F882A, MB90F882AS, MB90F883, MB90F883S, MB90F883A, MB90F883AS, MB90F883B, MB90F883BS, MB90F883BH, MB90F883BHS, MB90F883C, MB90F883CS, MB90F884, MB90F884S, MB90F884A, MB90F884AS, MB90F884B, MB90F884BS, MB90F884BH, MB90F884BHS, MB90F884C, MB90F884CS,
16 bit	MB90920 series	MB90F922NA, MB90F922NAS, MB90F922NB, MB90F922NBS, MB90F922NC, MB90F922NCS, MB90F923NC, MB90F923NCS, MB90F924NC, MB90F924NCS
16 bit	MB90950 series	MB90F952J, MB90F952JS, MB90F952JA, MB90F952JAS, MB90F952JB, MB90F952JBS, MB90F952JD, MB90F952JDS, MB90F952MB, MB90F952MBS, MB90F952MD, MB90F952MDS
16 bit	MB90990 series	MB90F997JA, MB90F997JAS, MB90F997JBS, MB90F997MA, MB90F997MAS, MB90F997MB, MB90F997MBS
16 bit	MB96xxx series	All 16FX Flash MCUs (MB96Fxxx)
32 bit	MB91210 series	MB91F211B, MB91F213A, MB91F218S
32 bit	MB91310 series	MB91F313, MB91F313A, MB91F314A, MB91F318R, MB91F318S
32 bit	MB91460 series	All MB91460 Series Flash MCUs (MB91F46x)
32 bit	MB91470 series	MB91F475, MB91F478, MB91F479
32 bit	MB91480 series	MB91F482, MB91F487
32 bit	MB91610 series	MB91F610, MB91F610A
32 bit	MB91635 series	MB91F635, MB91F637, MB91F637A, MB91F637B, MB91F637AB, MB91F639, MB91F639A, MB91F639B, MB91F639AB
32 bit	MB91640 series	MB91F644, MB91F647, MB91F644A, MB91F647A
32 bit	MB91660 series	MB91F662

5 Workaround

Please take any of the following measures to ensure proper erase sector functionality.

5.1 Polling that uses DQ6 (TOGGLE) toggle bit algorithm

Please judge the state of an automatic algorithm by using DQ6 as shown in the figure below.

Like the data polling flag (DQ7), the toggle bit flag (DQ6) is a flag mainly used to indicate whether the automatic algorithm is being executed or has ended. In the case of the toggle bit flag, a toggle bit function is used for that purpose.

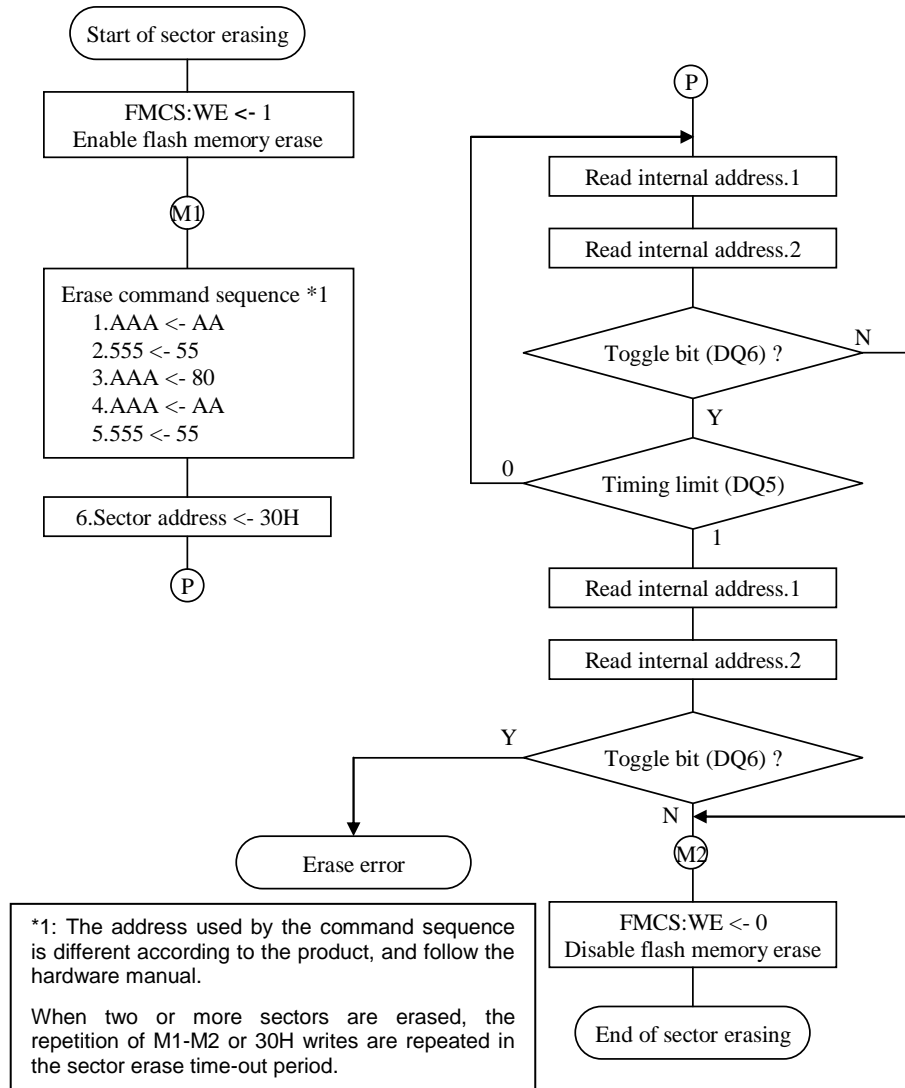


Figure 2: Workaround by DQ6

5.2 Start the polling of DQ7 after the sector erase time-out period passes

As shown in the timing chart of Figure 1, start the polling of DQ7 after waiting for 160us or more with software after the command is issued or waiting for DQ3 = 1 (end of the sector erase time-out period).

Please judge the state of an automatic algorithm by using DQ3 as shown in the figure below.

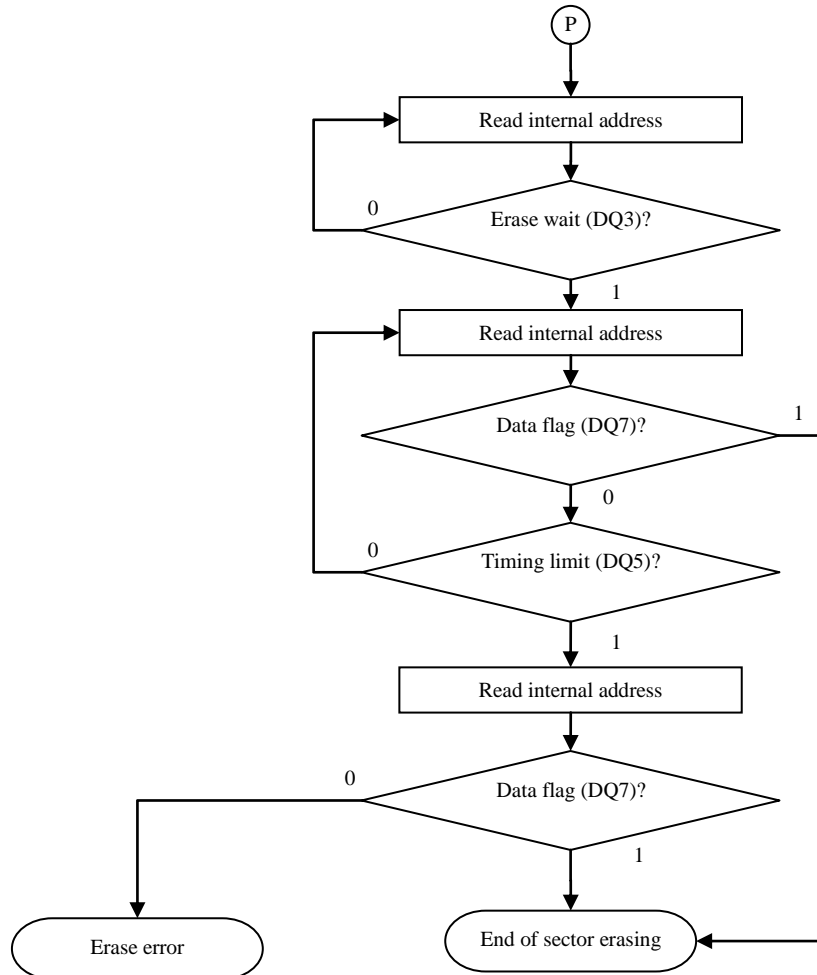


Figure 3: Workaround by DQ3

5.3 Data polling

Instead of polling only the DQ7 flag, all 8 data bits can be checked for equality to 1.

Please judge the state of an automatic algorithm by using data polling as shown in the figure below.

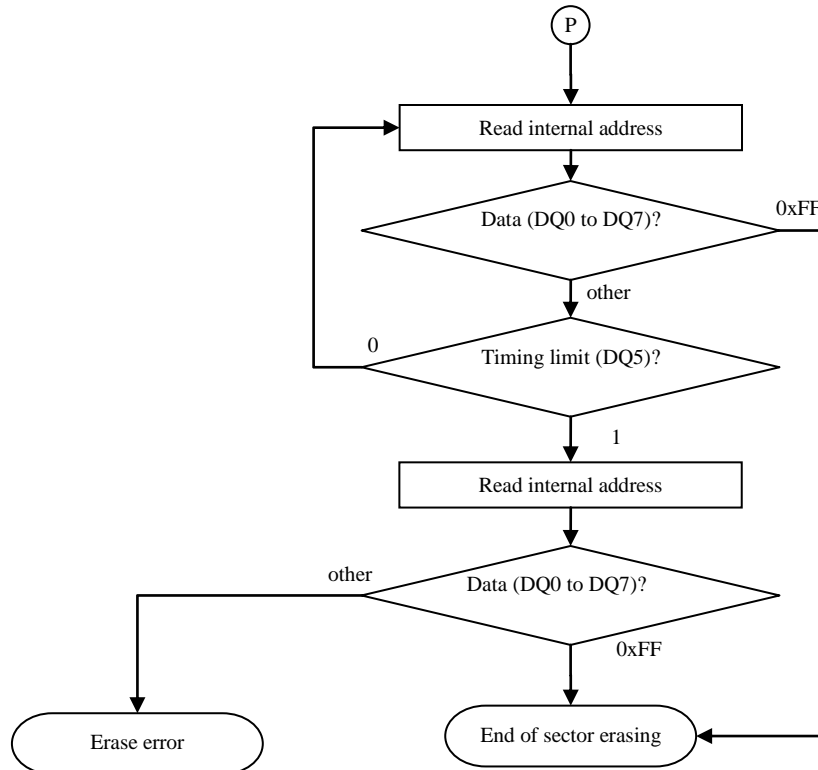


Figure 4: Workaround by Data Polling

5.4 MB96Fxxx Series (16FX)

The DQ7 state description during ‘sector erase wait’ state was corrected in the hardware manual MB96300 rev13. The examples given in earlier revisions were already showing use of correct sequence.

In the version MB96300 rev16, the complete Flash chapter was reworked to improve the comprehensibility, especially regarding the hardware sequence flags. Customers using the hardware sequence flags should read the updated Flash chapter of the MB96300 rev16 hardware manual and confirm that the flags are used in accordance to these descriptions.

5.5 MB91F46x Series (FR)

The hardware manual version 1.21 describes the sector erase algorithm as following:

Section 54.7.2. ‘Auto Algorithm Commands’

Sector Erase:

‘...After a timeout of 50us since the last sector-erase command was written, sector erase begins. ...’

In section 54.7.5 'Sample Use of Hardware Sequence Flag', the procedure shown in figure 7-4 "Write/erase Determination Sequence Using Data-polling Function" does not apply to Flash Sector Erase.

Please note that in procedure shown in figure 7-5 'Write/erase Determination Sequence Using Toggle-bit Function', the second operation 'Read (D0 to D7)' must be executed twice for reliable detection of DQ6 toggle.