

32-BIT MICROCONTROLLER **MB91360 SERIES**

FUNCTIONAL LIMITATION
CAN INTERRUPT SETTING

2009-03-27



Revision History

| Date | Issue |
|------------|-----------------------|
| 2009-03-03 | V1.0, Initial Version |
| 2009-03-27 | V1.1 Released Version |
| | |

This document contains 10 pages.

Abbreviations:

| | |
|-----|--------------------------------------|
| FME | Fujitsu Microelectronics Europe GmbH |
| MCU | Microcontroller |

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Fujitsu does not bear any warranty in the case this handling note is not fully observed.

1 Problem Description

A problem was found in the CAN interrupt synchronizer module on 32bit MCUs of the MB91360 series. Under certain conditions there might be spurious interrupts caused by CAN IRQ events. This problem is called 'CAN Interrupt Setting'.

2 Problem Conditions

The problem may occur if all of the following conditions are met:

- Base clock > 32 MHz
- Divider of CLKT is ≥ 3 and result of division $CLKP/CLKT$ is not an integer value
- Increasing temperature (probability is increasing towards specified maximum operating temperature $T_a=85C$, or above outside specified temperature range)

3 Affected Devices

The following devices are affected:

- All MB91360 series devices (all date codes)

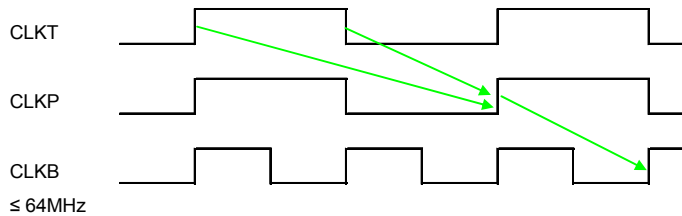
4 Affected Modules

This problem is affecting the interrupt generation consisting of:

- CAN interface (interrupt synchronizer)
- Interrupt Unit

5 Root Cause

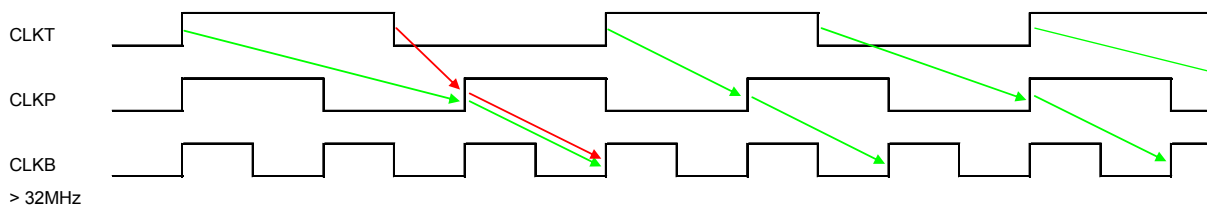
5.1 Correct function (e.g. configuration with CLKP:CLKT even divider):



There is no short path for $CLKB \leq 64MHz$ (green arrows).

CLKT is synchronizing CAN interrupts from CAN clock domain (asynchronous to core domain) to core clock domain, interrupts to Interrupt Unit (I-UNIT) are output on both rising edge and falling edge CLKT (due to IRQ latency performance). CLKP is capturing the interrupt signal within Interrupt Unit (I-UNIT) and providing Vector/Level to CPU (CLKB domain).

5.2 Incorrect function (e.g. configuration with CLKP:CLKT odd divider):



There is a short path for $CLKB > 32 MHz$ (upper red arrow).

Time between falling edge CLKT to rising edge CLKP is too short (upper red arrow), wrong Vector/Level might be provided to CPU, possibly causing wrong ISRs (of possible interrupt numbers 16-79 decimal) to be executed.

The occurrence of spurious interrupts is based on signal path delay between CAN interrupt synchronizer module and interrupt unit output registers. Therefore the probability of occurrence will increase with increasing temperature.

5.3 Affected clock division ratios

The problem can occur if base clock is > 32MHz, divider of CLK_T is ≥ 3 and result of division CLK_P/CLK_T is not an integer value.

The following table shows clock divider ratios which can cause the issue:

| | | | | | | | | | | | | | | | |
|-------------|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|
| CLK_P:CLK_T | 2:3 | | 4:3 | 5:3 | | 7:3 | 8:3 | | 10:3 | 11:3 | | 13:3 | 14:3 | | 16:3 |
| CLK_P:CLK_T | 2:5 | 3:5 | 4:5 | | 6:5 | 7:5 | 8:5 | 9:5 | | 11:5 | 12:5 | 13:5 | 14:5 | | 16:5 |
| CLK_P:CLK_T | 2:7 | 3:7 | 4:7 | 5:7 | 6:7 | | 8:7 | 9:7 | 10:7 | 11:7 | 12:7 | 13:7 | | 15:7 | 16:7 |
| CLK_P:CLK_T | 2:9 | 3:9 | 4:9 | 5:9 | 6:9 | 7:9 | 8:9 | | 10:9 | 11:9 | 12:9 | 13:9 | 14:9 | 15:9 | 16:9 |
| CLK_P:CLK_T | 2:11 | 3:11 | 4:11 | 5:11 | 6:11 | 7:11 | 8:11 | 9:11 | 10:11 | | 12:11 | 13:11 | 14:11 | 15:11 | 16:11 |
| CLK_P:CLK_T | 2:13 | 3:13 | 4:13 | 5:13 | 6:13 | 7:13 | 8:13 | 9:13 | 10:13 | 11:13 | 12:13 | | 14:13 | 15:13 | 16:13 |
| CLK_P:CLK_T | 2:15 | 3:15 | 4:15 | 5:15 | 6:15 | 7:15 | 8:15 | 9:15 | 10:15 | 11:15 | 12:15 | 13:15 | 14:15 | | 16:15 |

All other clock divider ratios not shown in the table do not cause any problem.

With clock divider ratios not shown in the table it is not necessary to use the proposed software workaround (even though, the workaround does not harm if used).

6 Workaround

6.1 Software workaround to avoid the occurrence of the problem

It is recommended to check existing application software using the table shown in “5.3 Affected clock division ratios” for possible existence of the problem.

In case an affected clock division ratio is used then using the following measure will completely avoid the occurrence of the problem:

- **Set register bits in CREG register E_INT = 1 and S_INT = 1**

Remark: It is recommended to use that setting for all new application software using a clock division ratio as shown in “5.3 Affected clock division ratios”.

The software workaround will completely resolve the problem.

6.2 CREG register description

CREG register (CAN0:0x10012D, CAN0:0x10032D, CAN0:0x10052D, CAN0:0x10072D)

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------------|-------------------|-------|-------|-------|-------|-------|-------|-------|--------|
| Address: | 10012DH (CAN0) | E_INT | S_INT | C_INV | L_INV | C_CLK | L_CLK | SYNCH | CDSBLE |
| Read/write | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) |
| Initial/ Bootrom value | | (0) | (0) | (0) | (0) | (0) | (0/1) | (0/1) | (0) |

Explanation of E_INT and S_SINT register function:

S_INT : Output interrupts on single edge / both edges (CLKT)

S_INT = 0 : Output interrupts on both edges (E_INT is don't care)

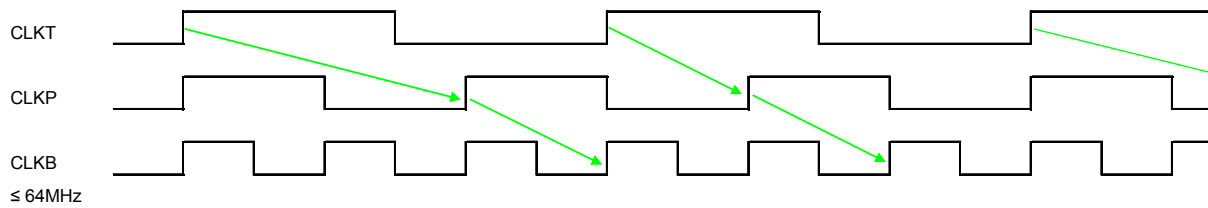
S_INT = 1 : Output interrupts on single edge (edge selection acc. to E_INT)

E_INT : Edge selection on single edge mode

E_INT = 0 : Output interrupts on falling edge CLKT

E_INT = 1 : Output interrupts on rising edge CLKT

6.3 Workaround function (e.g. configuration with CLKP:CLKT odd divider):



There is no short path for $CLKB \leq 64MHz$.

Interrupts are only output with rising edge CLKT to Interrupt Unit (CLKP domain) - a short path between CLKT and CLKP is prevented.

Drawback of the proposed workaround is the slightly higher interrupt latency. But it is judged as negligible for small division ratios of CLKP and CLKT. In above's example with $CLKB:CLKP:CLKT = 1:2:3$ there are only a maximum of 2 additional core clocks (CLKB) necessary.

7 Corrective action by Fujitsu

Fujitsu will add the description of affected clock division ratios and the related setting of E_INT and S_INT to the errata sheet and hardware manual of MB91360 series.