

**Fujitsu Microelectronics Europe**  
Functional Limitation Report

F<sup>2</sup>MC-16LX FAMILY  
16-BIT MICROCONTROLLER  
**MB90335 Series**

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FUNCTIONAL LIMITATION  
USB REPORT  
2008-07-29



Revision History

Date	Issue
2008-07-29	V1.0 initial version

This document contains 10 pages.

Abbreviations:

FME            Fujitsu Microelectronics Europe GmbH  
 MCU            Microcontroller

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**Fujitsu does not bear any warranty in the case this handling note  
is not fully observed.**

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**Report on USB Function Specification Limitation of MB90335 series and MB90330A series**

Thank you very much for your continued loyalty to us.

We will report usage limitations on the USB function of MB90335 series and MB90330A series as follows. Please be sure to take adequate notice of the issues reported.

Regards,

--- Note---

## 1 Target products

MB90335 series : MB90V330A, MB90F337, MB90337

MB90330A series: MB90V330A, MB90F334A, MB90333A

## 2 Contents of specification limitations

This USB function was developed based on the USB 1.1 standard before the USB 2.0 standard was released. Therefore, the following two specification limitations are found which have not been specified by the USB 1.1 standard.

### (1) Specification limitation on isochronous transfer

In the isochronous transfer of USB 2.0, the item which specifies the initial settings where Alternate value is 0 and the number of maximum packets is 0 was added to the specification. In this USB function, STALL response is automatically given to the host when Alternate value is tried to set to a value other than 0 with the Alternate interface setting command from the host. Therefore, the Alternate value cannot be changed. So, the number of maximum packets cannot be changed with the Alternate value.

### (2) STALL response release specification limitation of end point 0

For a device which does not support the newly added commands for High speed of USB 2.0, the STALL response is required for the newly added commands. Therefore, even at normal communication, the STALL response might be required. After the STALL response, when the corresponding command is received, it is necessary to release STALL (SETPbit =0) within the fixed time after STALL response detection (STALbit =1). Please refer to attached material for details.

### 3 Document revision schedule

Hereafter, we will revise the hardware manuals for changing this specification limitation on the following revision schedule. We will also add supplementary explanation on STALL of end point 1 to end point 5 with this revision.

Series name	Hardware manual revision schedule	
	(Japanese)	(English)
MB90335 series	By the middle of September, 2008	By the middle of September, 2008
MB90330A series	By the middle of September, 2008	By the middle of September, 2008

### 4 Attached materials

Attached material 1: "STALL response release specification limitation of end point 0"

Attached material 2: "Supplementary explanation on STALL response specification of end point 1 to end point 5"

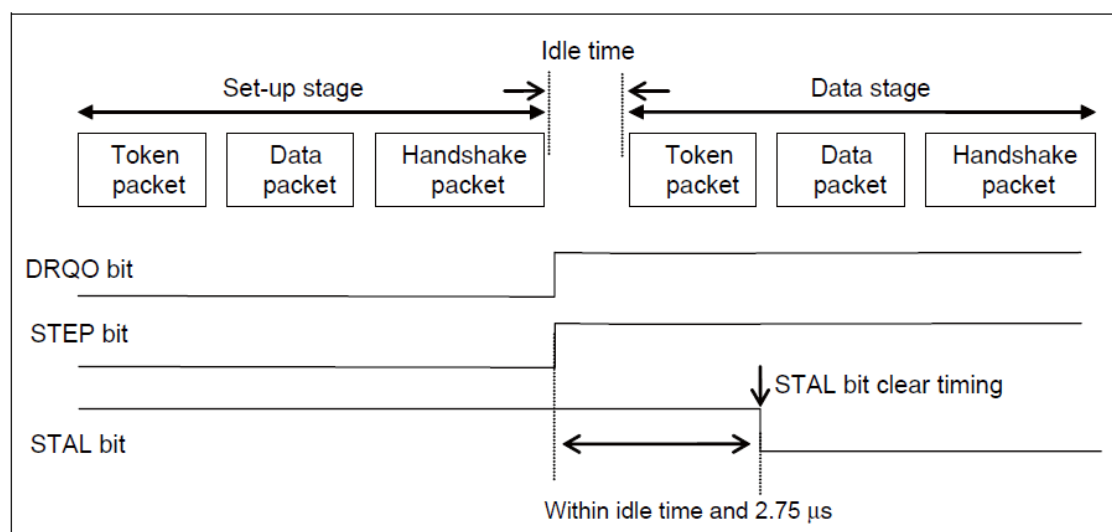
#### **STALL response release specification limitation of end point 0**

STALL response and release procedures for Endpoint0 are executed with STAL bit of EP0 Control Register (EP0C).

For STALL response, interprets the command at detecting SETP bit of "1" (DRQO bit = 1 for interrupt) that indicates the set-up stage of control transfer. After setting STAL bit, clear interrupt cause (DRQO bit).

For STALL release, clears STAL bit at detecting SETP bit of "1" (DRQO bit = 1 for interrupt) that indicates the set-up stage of control transfer, and sets STAL bit if the STALL response is required.(See Figure 1)

Figure 1. STAL Bit Clear Timing



For STALL response release (STAL bit clear), clear STAL bit the period between the time when STEP bit of "1" (DRQ0 bit= 1 for interrupt) is detected and the time when the data packet transmission/reception of the next data stage is started. The period between the time when DRQ0 becomes "1" and the time when STAL bit is cleared is as follows: (Transfer speed: at Full speed of 12Mbps) When STAL bit is not cleared in the following period, execute STAL response with the handshake of data stage.

The period between the time when DRQ0 BIT of "1" is detected and the time when STAL bit is cleared:

within idle time + 2.75  $\mu$ s

\* When idle time is the shortest period of 2-bit transfer time, the above period is within about 2.9  $\mu$ s.

If the STAL bit clear cannot be executed within the above period, take appropriate countermeasures such as lengthening of the idle time with a driver of USB host.

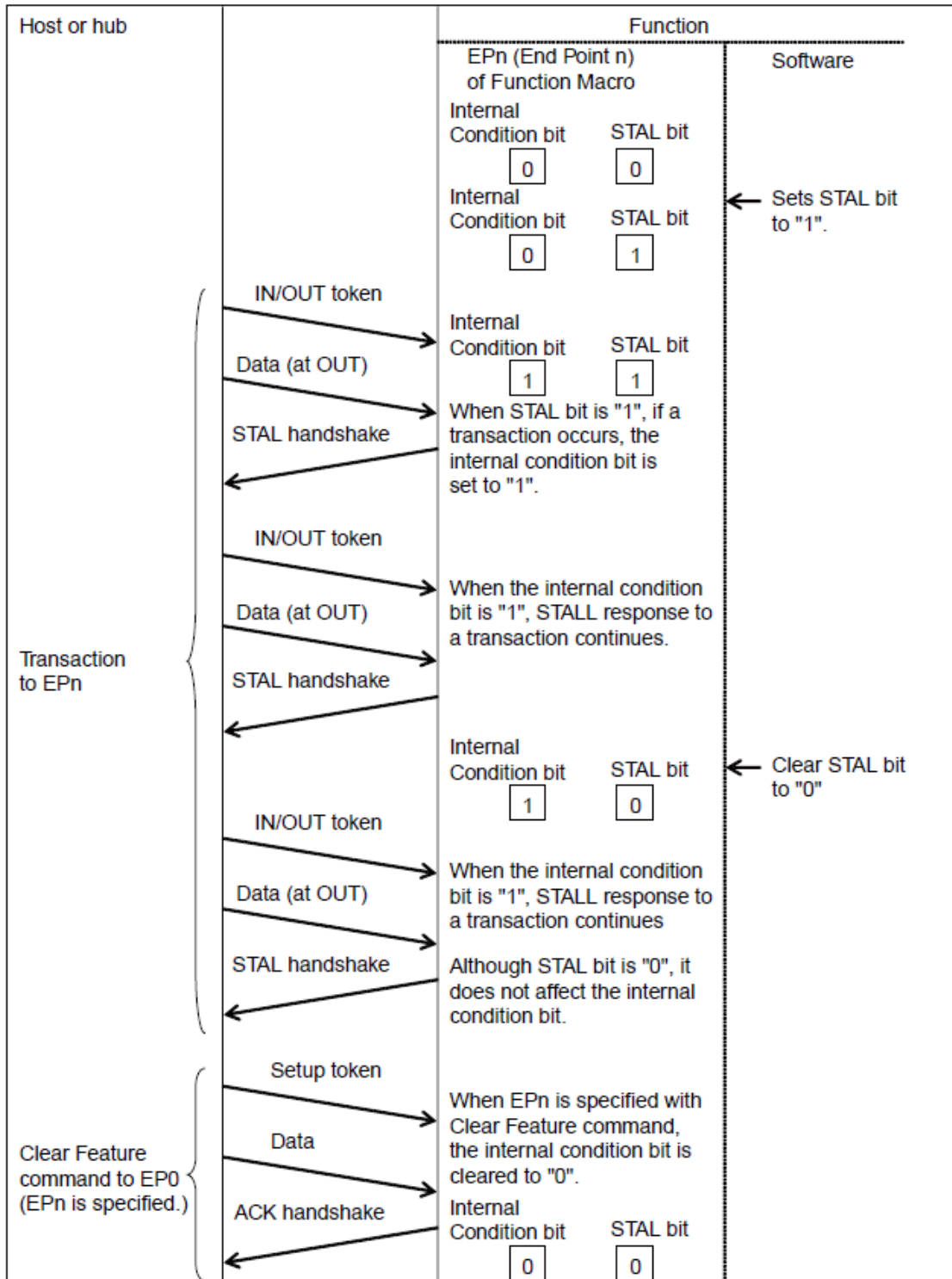
### **Supplementary explanation on STALL response specification of end point 1 to end point 5**

STALL response /release of Endpoints 1 to 5 are controlled with Control registers of EP1 to EP5 and internal condition bit

#### **1. To execute STAL response with software**

The procedures to execute STAL response with software are shown in Figure 1. To execute STAL response, set STAL bit of the relevant endpoint with software. In this time, the internal condition bit does not change. Furthermore, when a host generates a transaction to the endpoint where STAL bit is set, hardware would automatically set the internal condition bit of the relevant endpoint and give STALL response to the host. Once the internal condition bit is set, the internal condition bit has been set and continues STAL response until Clear Feature command is issued from the host despite of the clearing of STAL bit. As long as the STAL bit is set, STAL bit response continues even if the internal condition bit is cleared with Clear Feature command because the internal condition bit is set every time a transaction to the relevant endpoint occurs. Therefore, to release the STAL response, be sure to clear STAL bit and the internal condition bit with the Clear Feature command.

Figure 1 Case where STALL response is executed with software processing



## 2. To automatically execute STALL response with hardware.

The procedures to execute STALL response with hardware are shown in Figure 2. When STALL response is set with Set Feature command, the hardware would automatically set the internal condition bit of the relevant endpoint and gives the STALL response regardless of the STAL bit. Once the internal condition bit is set, the internal condition bit has been held until Clear Feature command is issued from the host to clear the internal condition bit regardless of STAL bit. After the relevant bit is cleared with Clear Feature command, STAL bit is referenced. Therefore, to clear STALL response, be sure to clear the internal condition bit with Clear Feature command.

Figure 2 Case where STALL response is executed with hardware automatically

